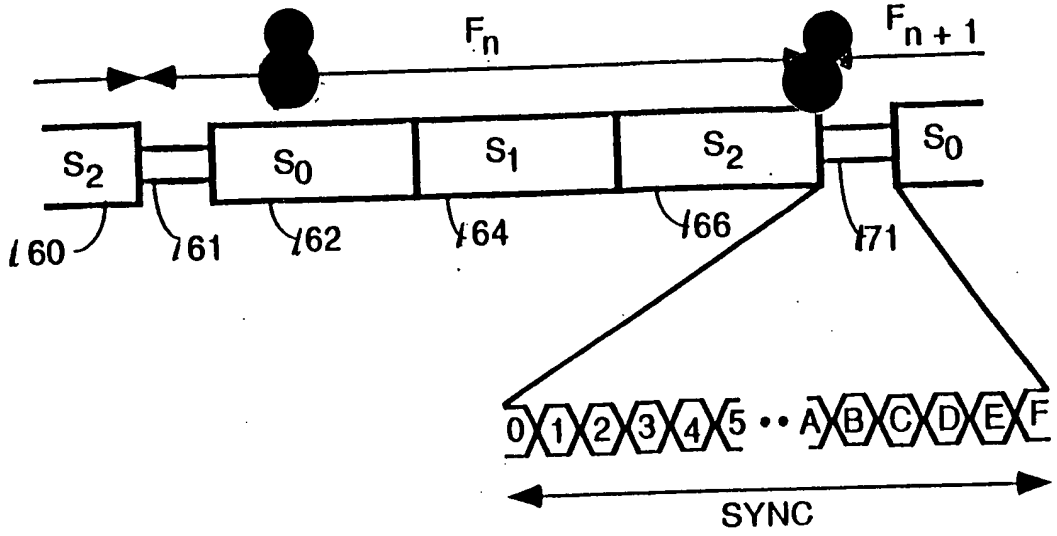

F_n
F_{n+1}
S_2
S_0
S_1
S_2
S_0
160
161
162
164
166
171
0 1 2 3 4 5 • • A B C D E F
SYNC

FIG. 4A

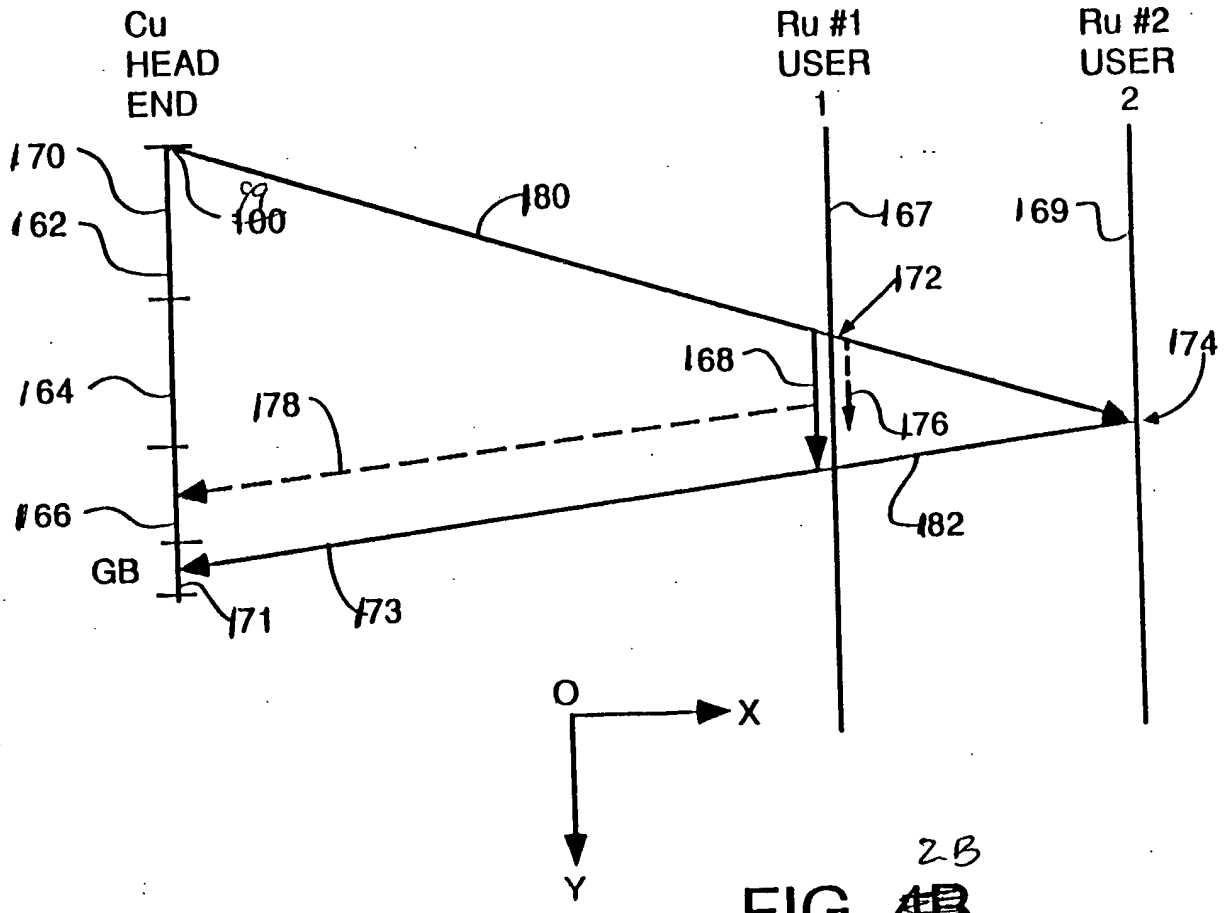

Cu
HEAD
END
Ru #1
USER
1
Ru #2
USER
2
170
162
164
166
GB
171
173
100
180
167
169
172
168
174
176
178
182
O
X
Y

FIG. 4B

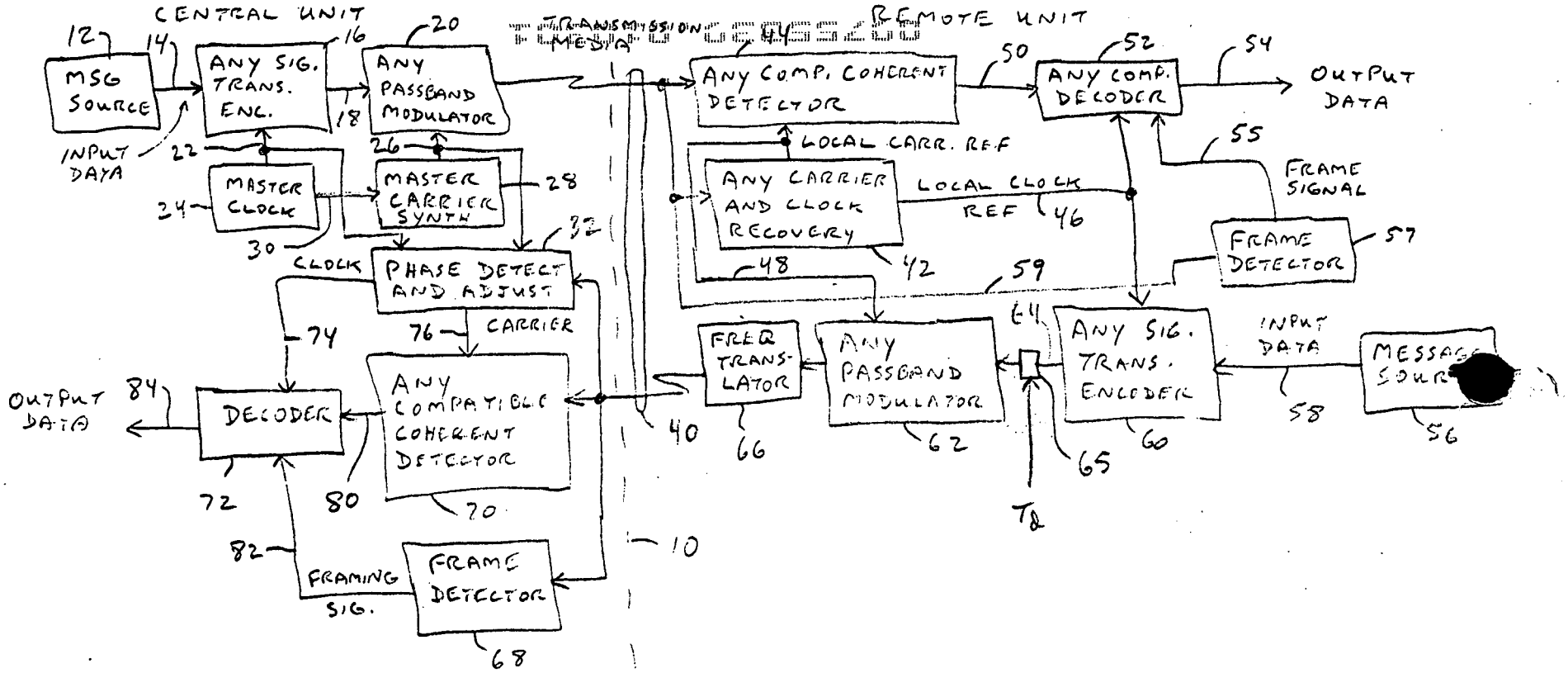

CENTRAL UNIT
REMOTE UNIT
TRANSMISSION MEDIA
12
14
16
18
20
MSG SOURCE
ANY SIG. TRANS. ENC.
ANY PASSBAND MODULATOR
INPUT DATA
22
26
MASTER CLOCK
MASTER CARRIER SYNTH
24
28
30
32
CLOCK
PHASE DETECT AND ADJUST
74
76
CARRIER
OUTPUT DATA
84
DECODER
ANY COMPATIBLE COHERENT DETECTOR
72
80
70
82
FRAMING SIG.
FRAME DETECTOR
68
10
40
FREQ TRANS-LATOR
66
ANY PASSBAND MODULATOR
62
64
65
ANY SIG. TRANS. ENCODER
60
INPUT DATA
58
MESSAGE SOURCE
56
T_R
ANY COMP. COHERENT DETECTOR
50
ANY COMP. DECODER
52
54
OUTPUT DATA
LOCAL CARR. REF
ANY CARRIER AND CLOCK RECOVERY
42
48
LOCAL CLOCK REF
46
55
FRAME SIGNAL
FRAME DETECTOR
57
59

FIG. 1

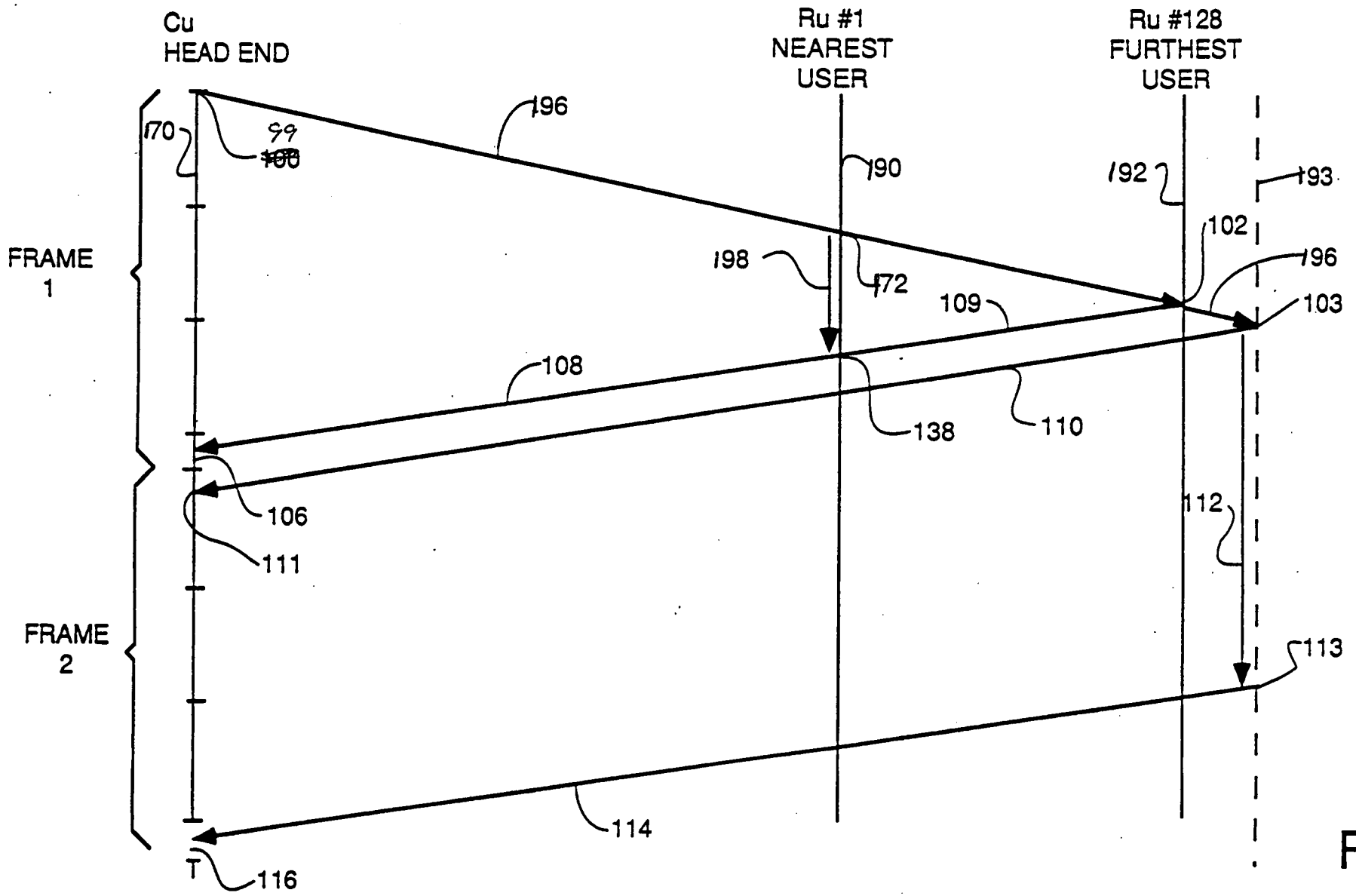


FIG. 5

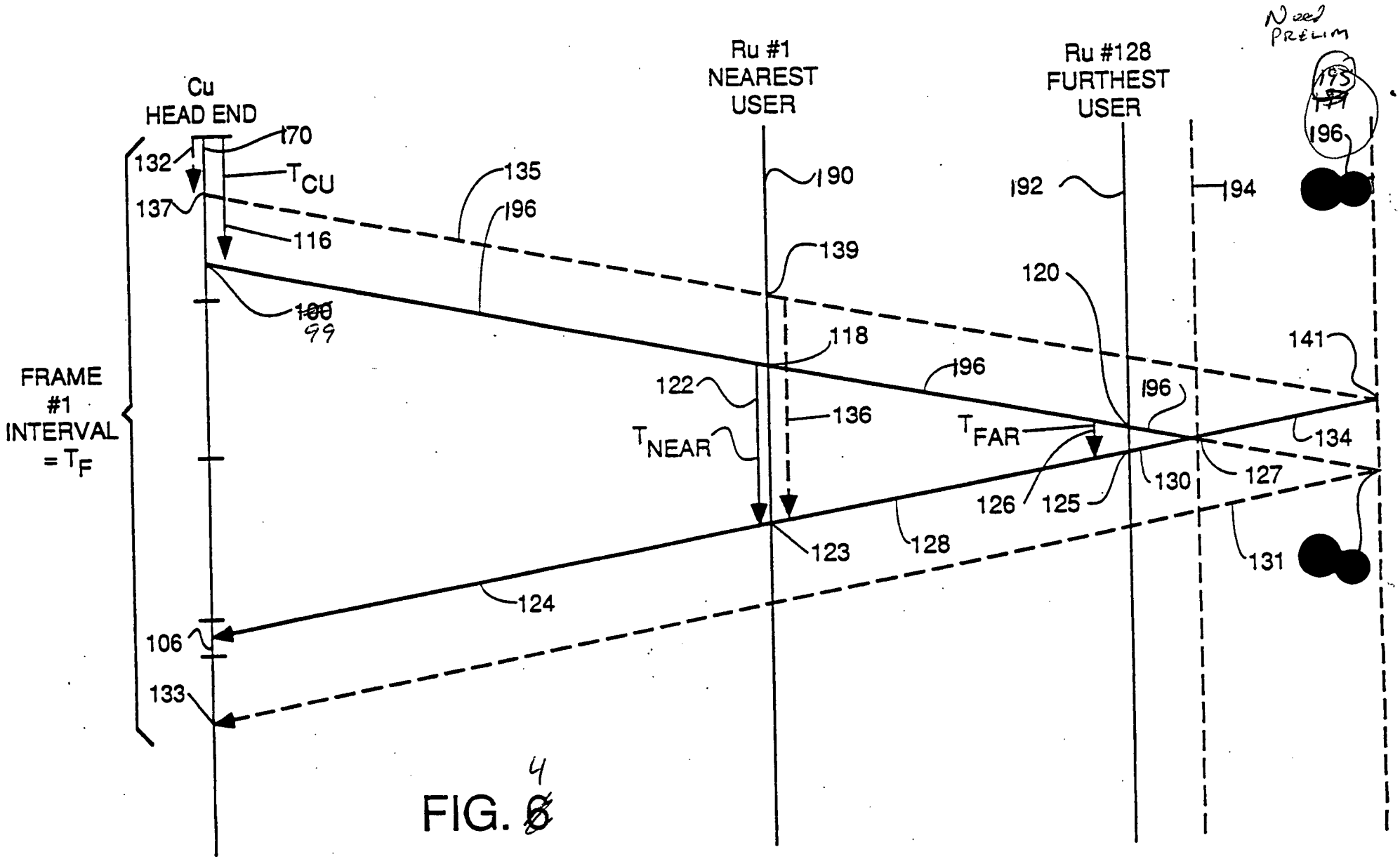
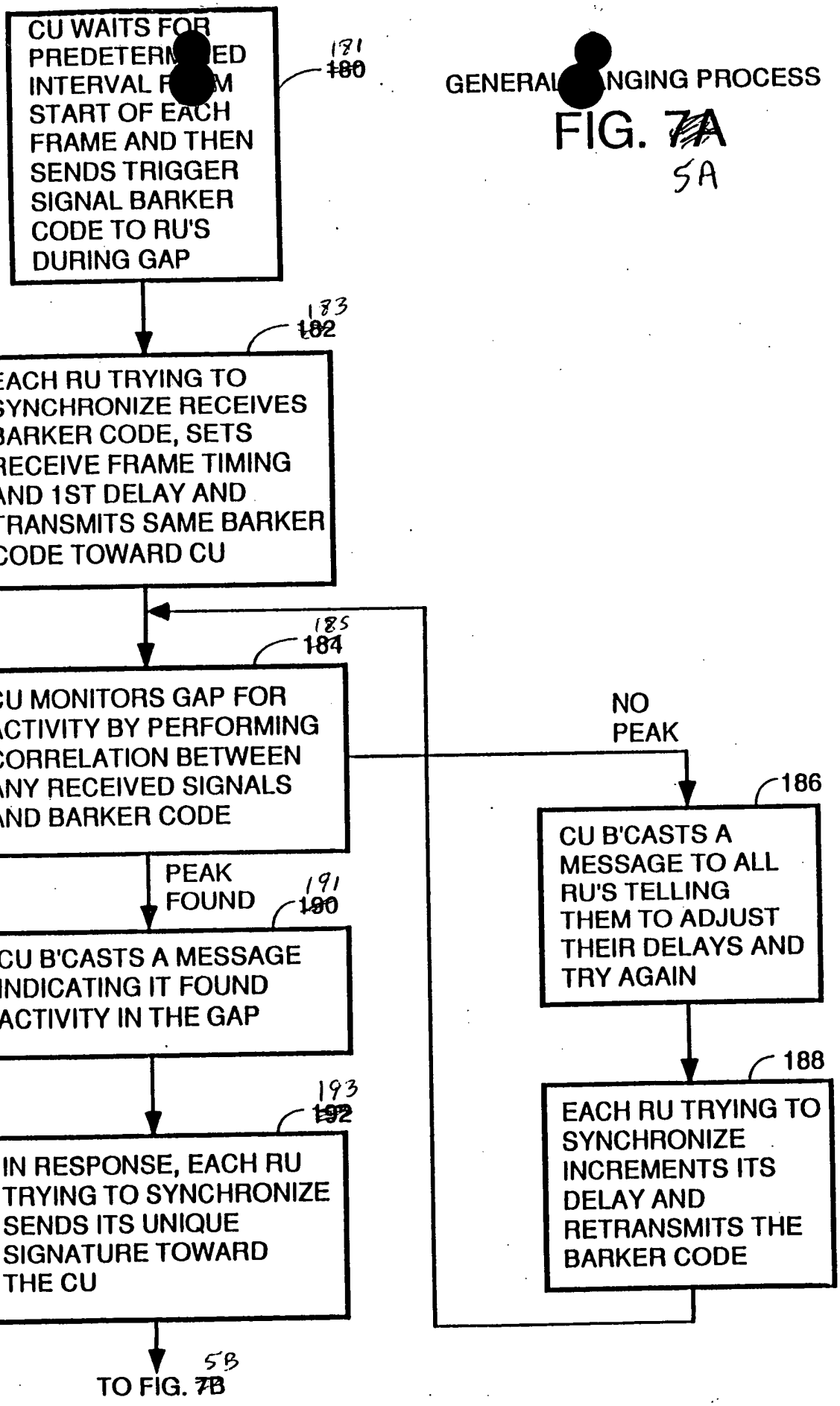


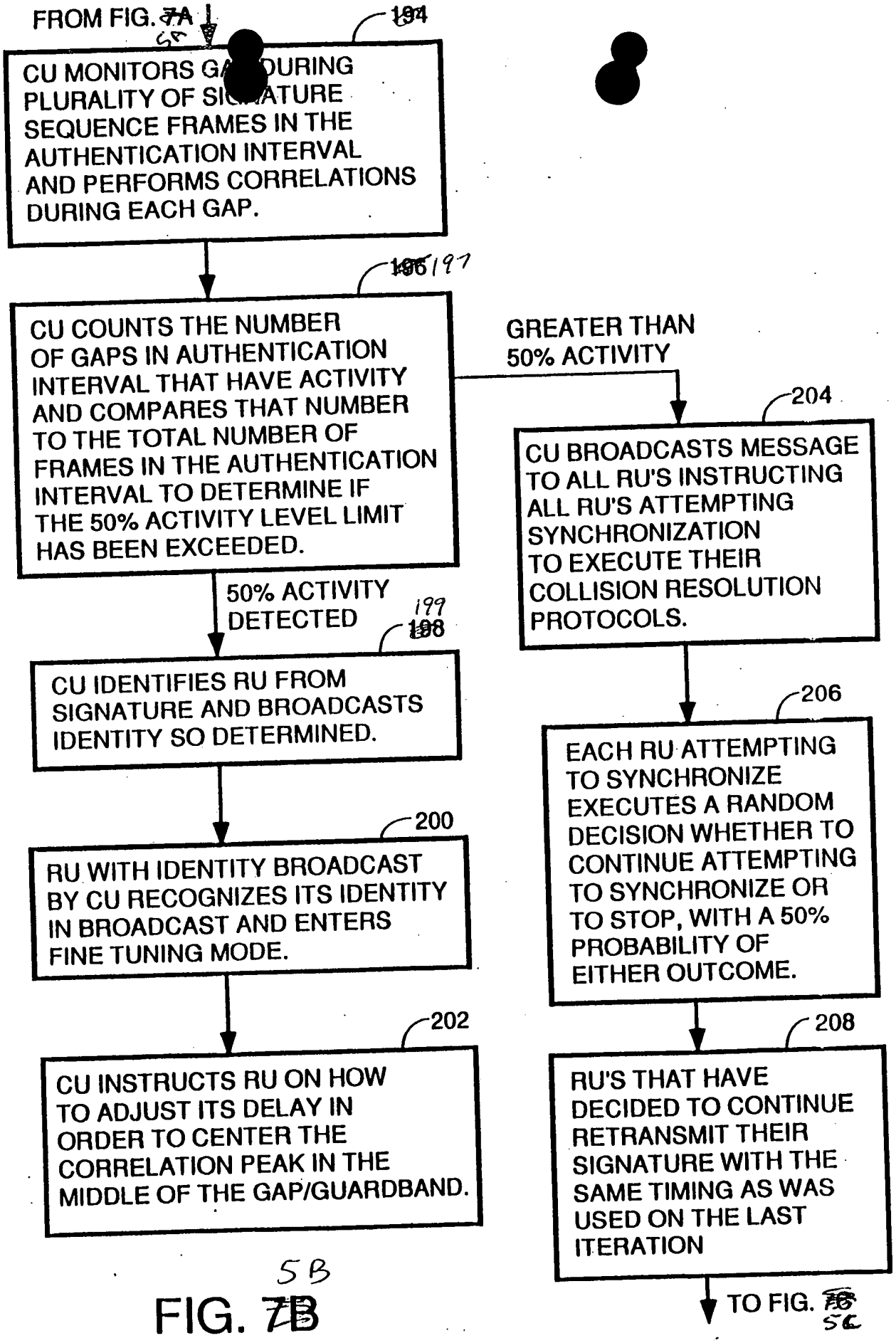
FIG. 4

GENERAL RANGING PROCESS

FIG. 7A

5A




FROM FIG. 7A
194
CU MONITORS GAPS DURING PLURALITY OF SIGNATURE SEQUENCE FRAMES IN THE AUTHENTICATION INTERVAL AND PERFORMS CORRELATIONS DURING EACH GAP.
196/197
CU COUNTS THE NUMBER OF GAPS IN AUTHENTICATION INTERVAL THAT HAVE ACTIVITY AND COMPARES THAT NUMBER TO THE TOTAL NUMBER OF FRAMES IN THE AUTHENTICATION INTERVAL TO DETERMINE IF THE 50% ACTIVITY LEVEL LIMIT HAS BEEN EXCEEDED.
GREATER THAN 50% ACTIVITY
204
CU BROADCASTS MESSAGE TO ALL RU'S INSTRUCTING ALL RU'S ATTEMPTING SYNCHRONIZATION TO EXECUTE THEIR COLLISION RESOLUTION PROTOCOLS.
50% ACTIVITY DETECTED
199
198
CU IDENTIFIES RU FROM SIGNATURE AND BROADCASTS IDENTITY SO DETERMINED.
206
EACH RU ATTEMPTING TO SYNCHRONIZE EXECUTES A RANDOM DECISION WHETHER TO CONTINUE ATTEMPTING TO SYNCHRONIZE OR TO STOP, WITH A 50% PROBABILITY OF EITHER OUTCOME.
200
RU WITH IDENTITY BROADCAST BY CU RECOGNIZES ITS IDENTITY IN BROADCAST AND ENTERS FINE TUNING MODE.
202
CU INSTRUCTS RU ON HOW TO ADJUST ITS DELAY IN ORDER TO CENTER THE CORRELATION PEAK IN THE MIDDLE OF THE GAP/GUARDBAND.
208
RU'S THAT HAVE DECIDED TO CONTINUE RETRANSMIT THEIR SIGNATURE WITH THE SAME TIMING AS WAS USED ON THE LAST ITERATION
TO FIG. 7B 5C

5B

FIG. 7B

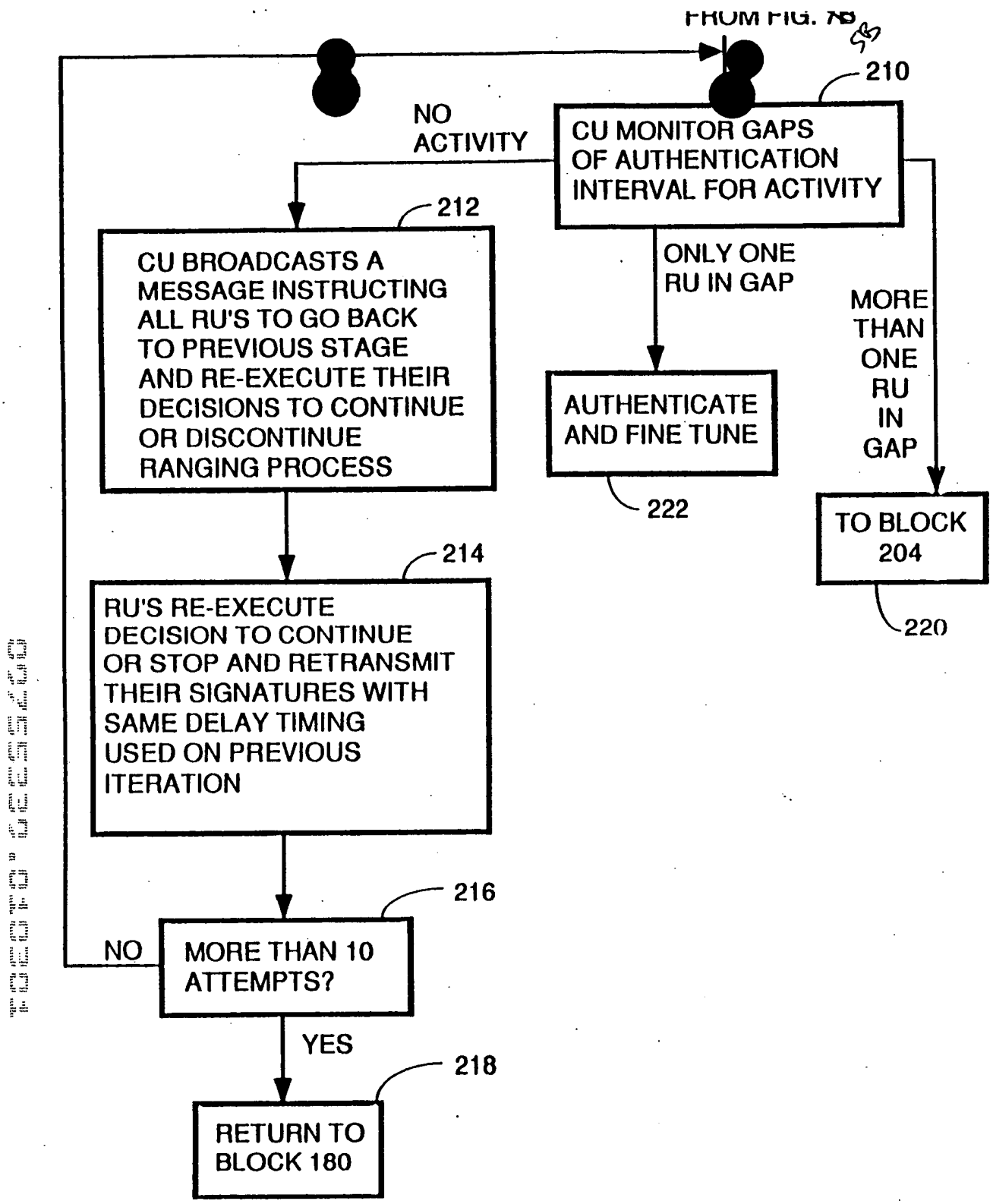
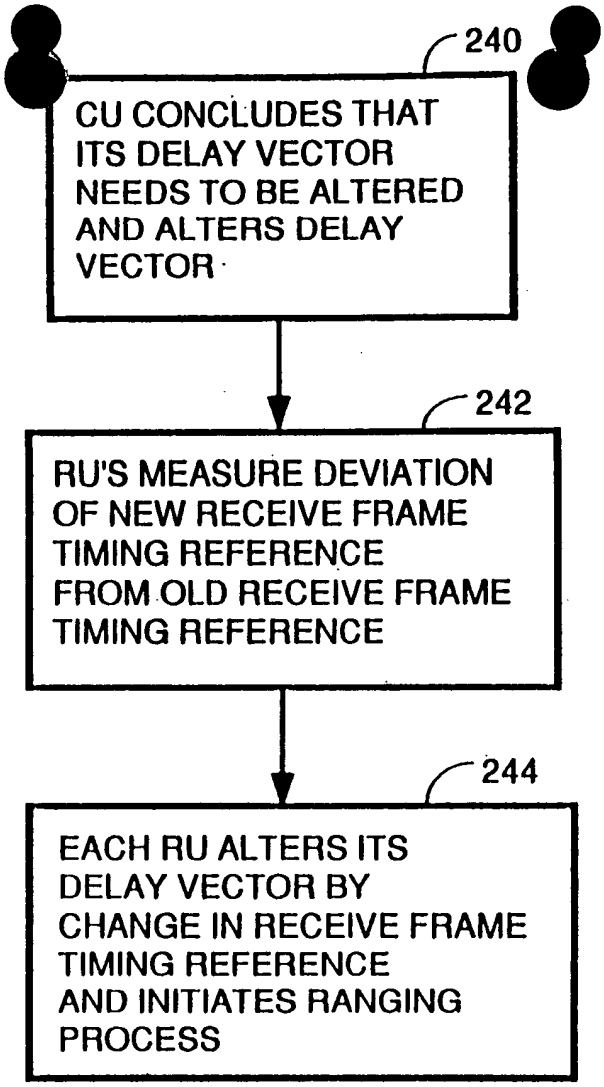

FROM FIG. 7B
210
CU MONITOR GAPS OF AUTHENTICATION INTERVAL FOR ACTIVITY
NO ACTIVITY
212
CU BROADCASTS A MESSAGE INSTRUCTING ALL RU'S TO GO BACK TO PREVIOUS STAGE AND RE-EXECUTE THEIR DECISIONS TO CONTINUE OR DISCONTINUE RANGING PROCESS
ONLY ONE RU IN GAP
AUTHENTICATE AND FINE TUNE
222
MORE THAN ONE RU IN GAP
TO BLOCK 204
220
214
RU'S RE-EXECUTE DECISION TO CONTINUE OR STOP AND RETRANSMIT THEIR SIGNATURES WITH SAME DELAY TIMING USED ON PREVIOUS ITERATION
216
NO
MORE THAN 10 ATTEMPTS?
YES
218
RETURN TO BLOCK 180

FIG. 7C



6

FIG. 8

DEAD RECKONING RE-SYNC

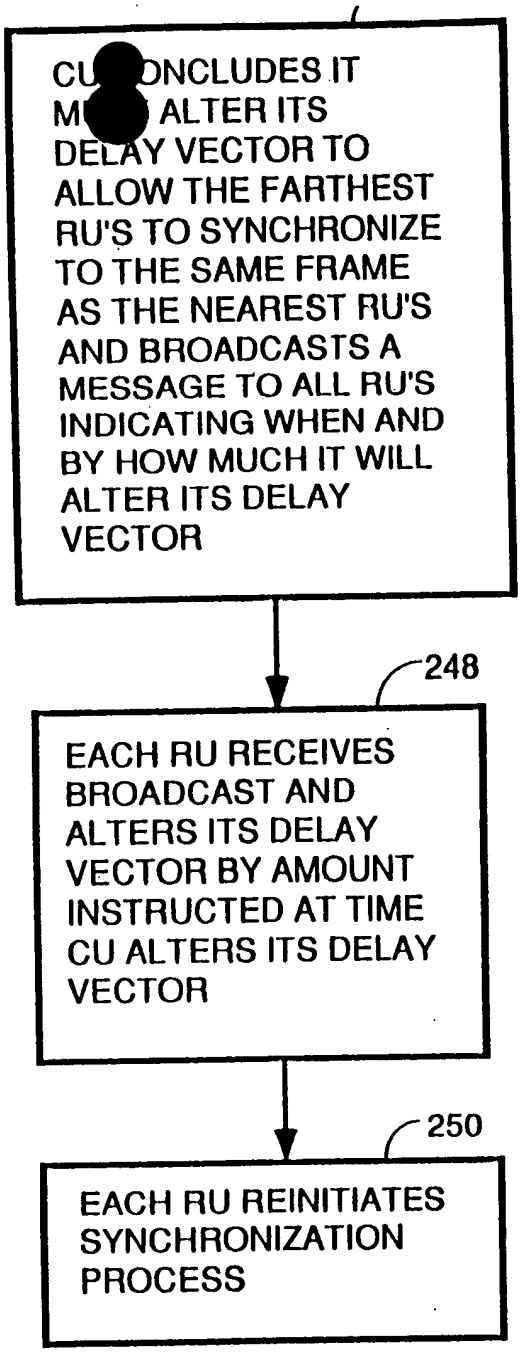


FIG. 9

PRECURSOR EMBODIMENT

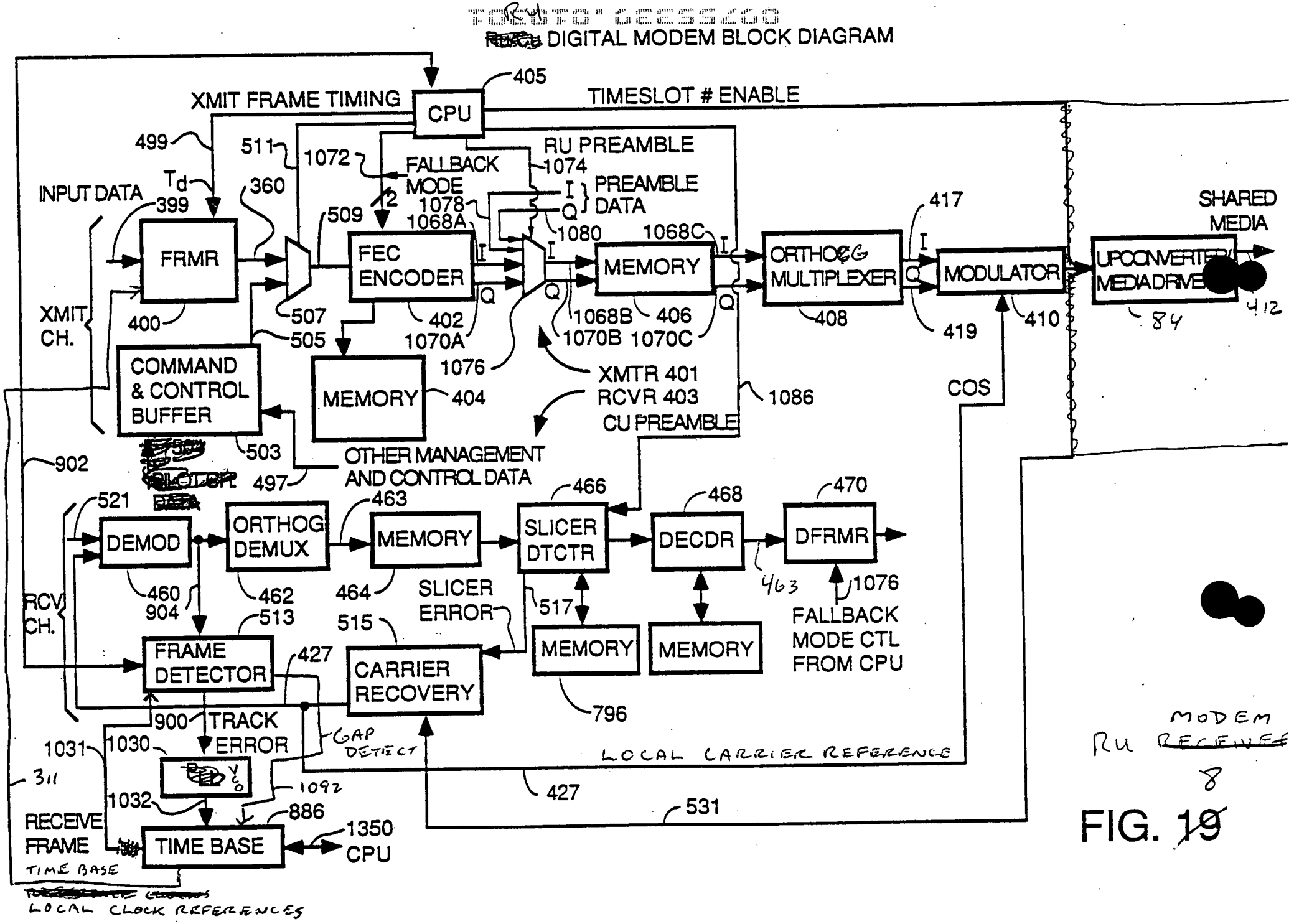

DIGITAL MODEM BLOCK DIAGRAM
XMIT FRAME TIMING
CPU
405
TIMESLOT # ENABLE
499
511
1072
FALLBACK MODE
RU PREAMBLE
1074
PREAMBLE DATA
INPUT DATA
Td
399
360
509
1078
1068A
1080
1068C
417
SHARED MEDIA
FRMR
FEC ENCODER
MEMORY
ORTHOG MULTIPLEXER
MODULATOR
UPCONVERTER/ MEDIADRIVE
412
84
XMIT CH.
400
507
505
402
1070A
1068B
406
1070B 1070C
408
419
410
COMMAND & CONTROL BUFFER
MEMORY
404
1076
XMTR 401
RCVR 403
CU PREAMBLE
1086
COS
503
OTHER MANAGEMENT AND CONTROL DATA
497
902
521
463
466
468
470
DEMOD
ORTHOG DEMUX
MEMORY
SLICER DTCTR
DECDR
DFRMR
460
904
462
464
SLICER ERROR
517
463
1076
RCV CH.
513
515
FALLBACK MODE CTL FROM CPU
FRAME DETECTOR
427
CARRIER RECOVERY
MEMORY
MEMORY
796
900
TRACK ERROR
GAP DETECT
1031
1030
311
1092
1032
886
RECEIVE FRAME
TIME BASE
1350
CPU
TIME BASE
LOCAL CLOCK REFERENCES
LOCAL CARRIER REFERENCE
427
531
MODEM RU RECEIVE
8

FIG. 19

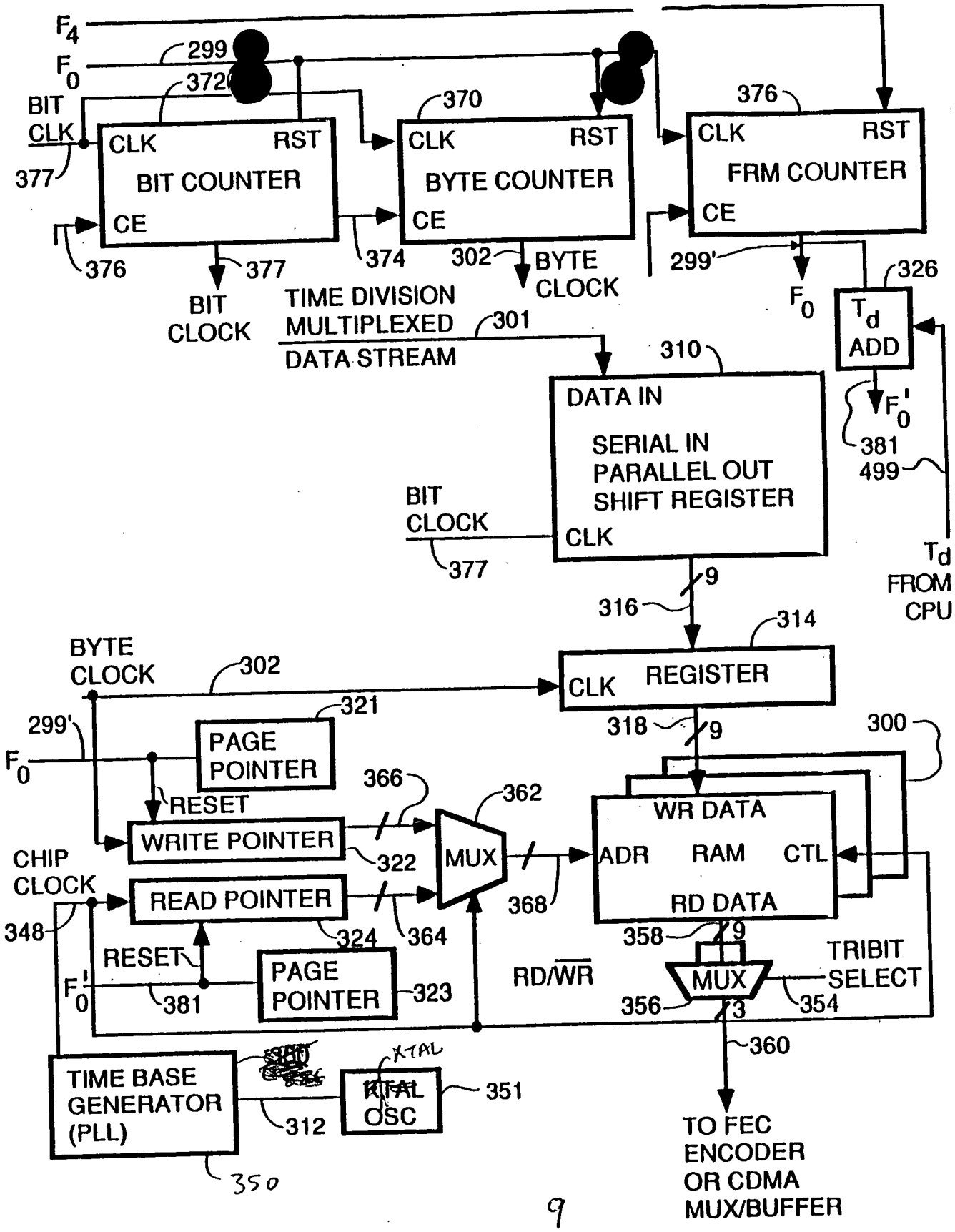

F4
F0
299
372
BIT CLK
377
CLK
RST
BIT COUNTER
CE
376
377
BIT CLOCK
374
370
CLK
RST
BYTE COUNTER
CE
302
BYTE CLOCK
376
CLK
RST
FRM COUNTER
CE
299'
F0
326
Td ADD
F0'
381
499
TIME DIVISION MULTIPLEXED DATA STREAM
301
310
DATA IN
SERIAL IN PARALLEL OUT SHIFT REGISTER
CLK
BIT CLOCK
377
9
316
Td FROM CPU
314
CLK REGISTER
BYTE CLOCK
302
318
9
300
299'
F0
321
PAGE POINTER
RESET
366
362
WRITE POINTER
322
MUX
WR DATA
ADR RAM CTL
RD DATA
CHIP CLOCK
348
READ POINTER
324
364
368
358
9
RESET
F0'
381
PAGE POINTER
323
RD/WR
MUX
TRIBIT SELECT
356
3
354
360
TIME BASE GENERATOR (PLL)
312
XTAL OSC
351
350
TO FEC ENCODER OR CDMA MUX/BUFFER

FIG. 12

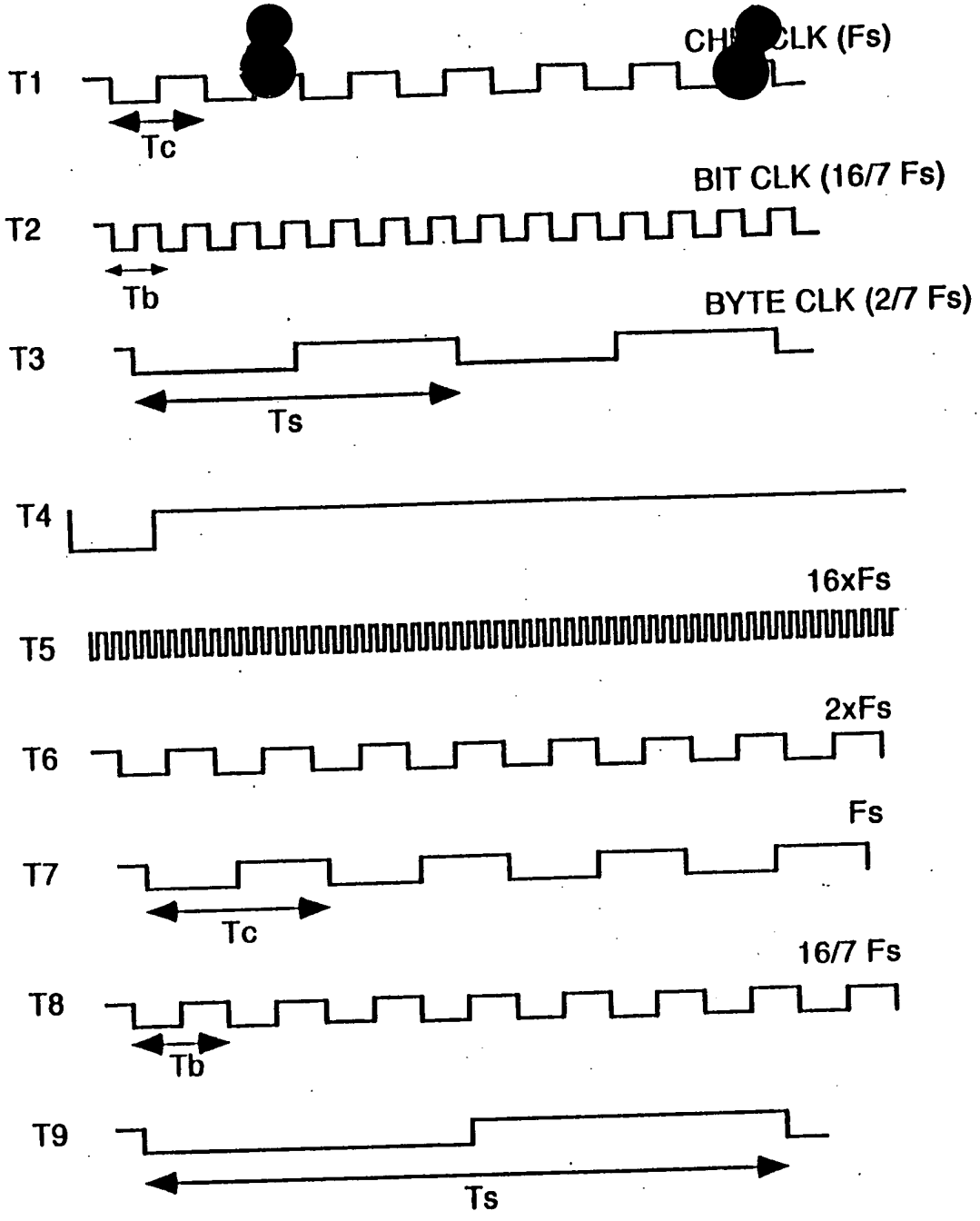
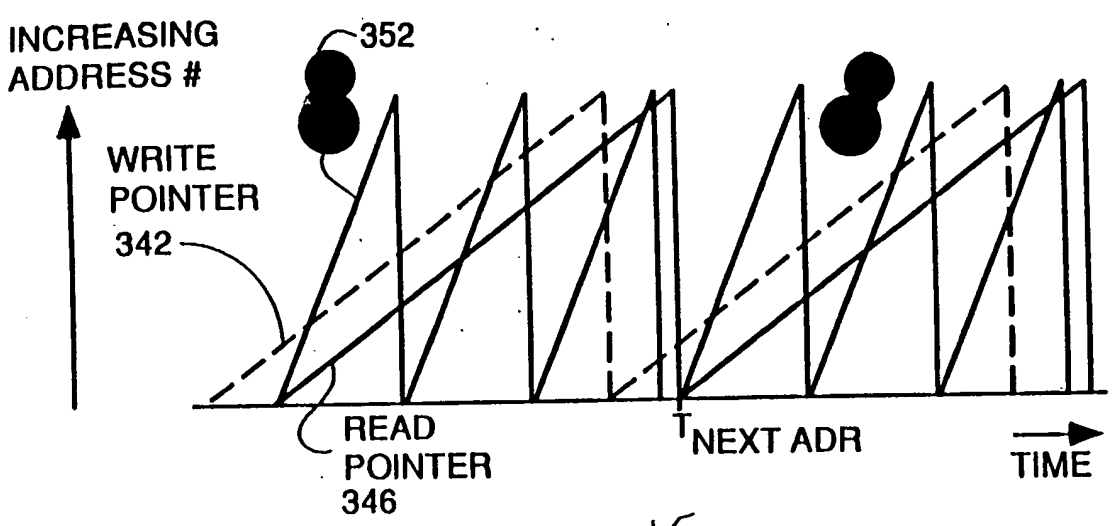
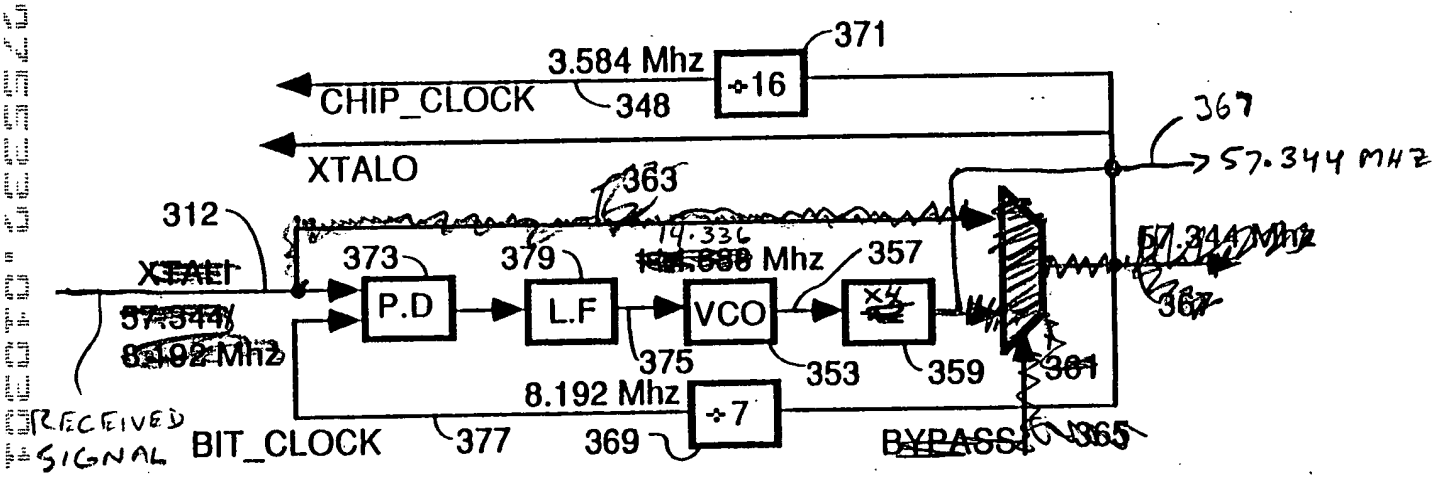

CH CLK (Fs)
T1
Tc
BIT CLK (16/7 Fs)
T2
Tb
BYTE CLK (2/7 Fs)
T3
Ts
T4
16xFs
T5
2xFs
T6
Fs
T7
Tc
16/7 Fs
T8
Tb
T9
Ts

FIG. 10/13



15

FIG. 17



11

FIG. 18

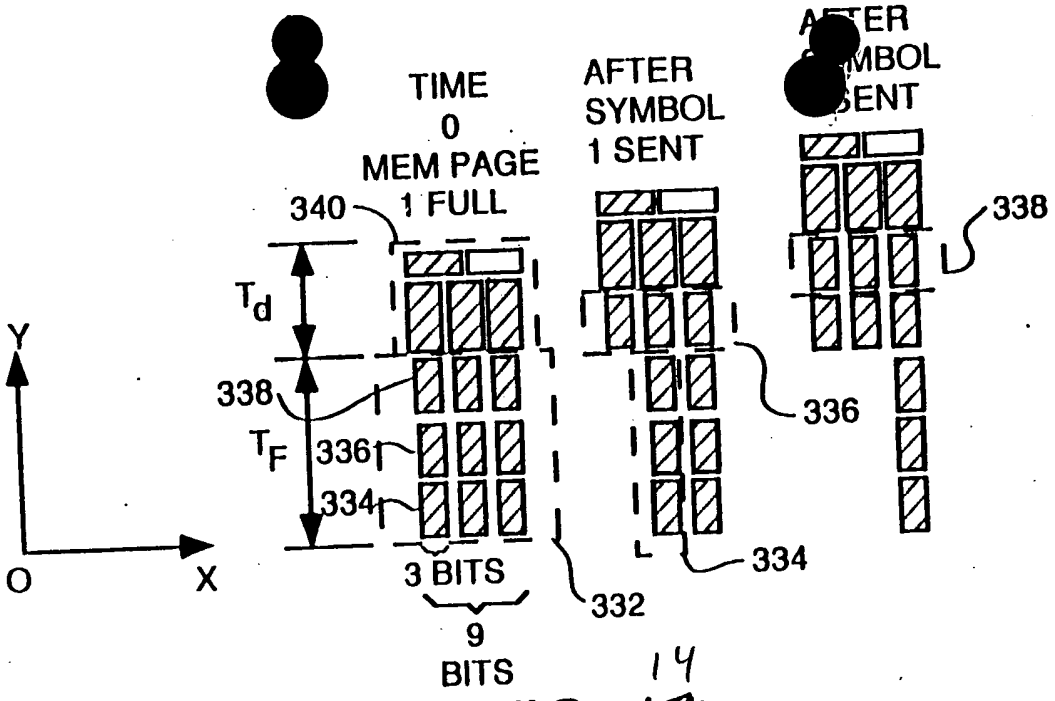


FIG. 14

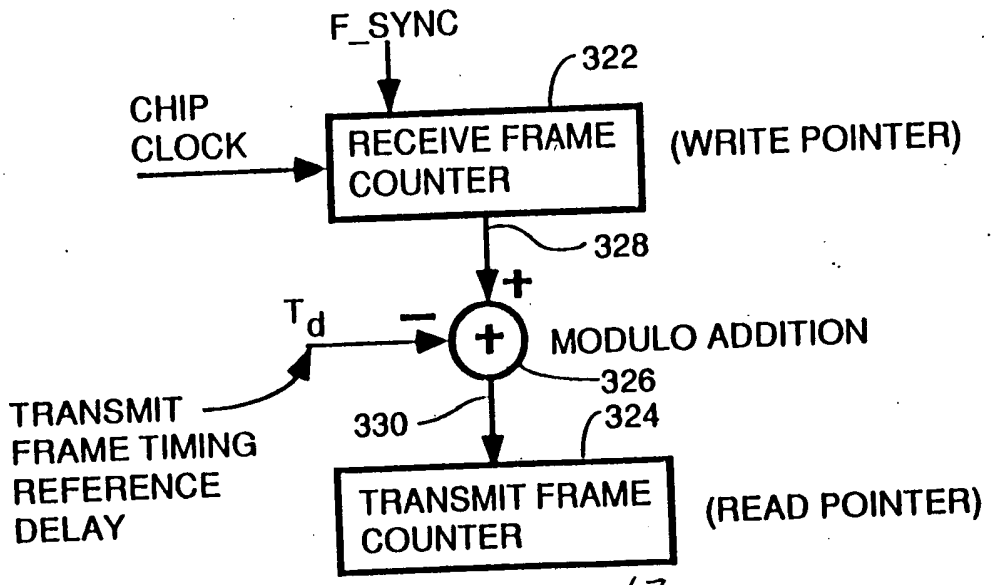


FIG. 15

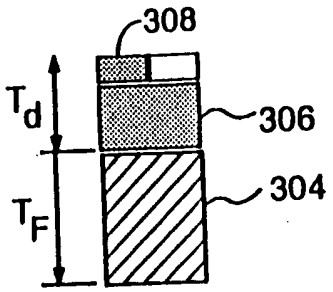


FIG. 16

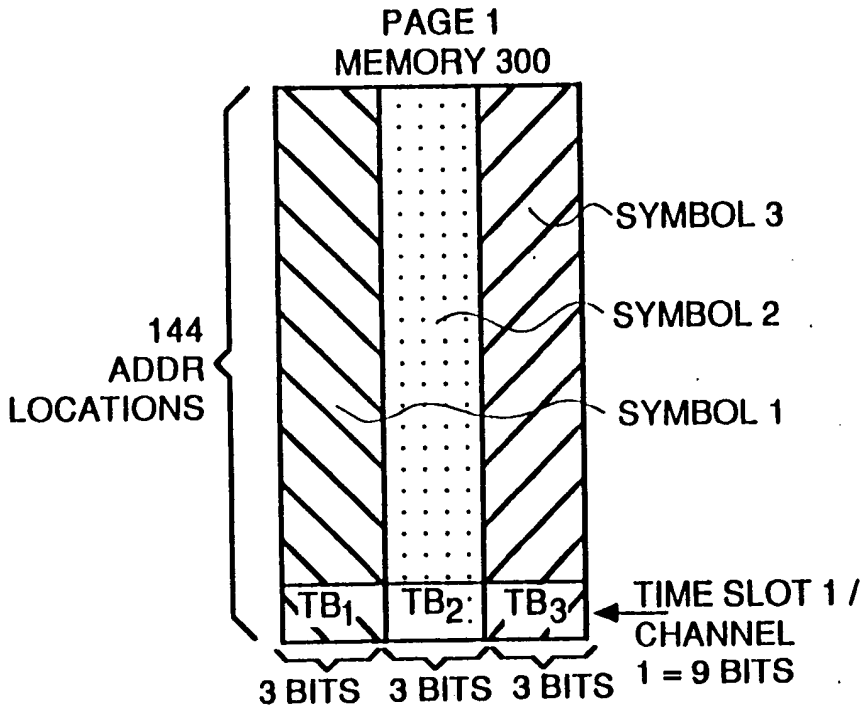
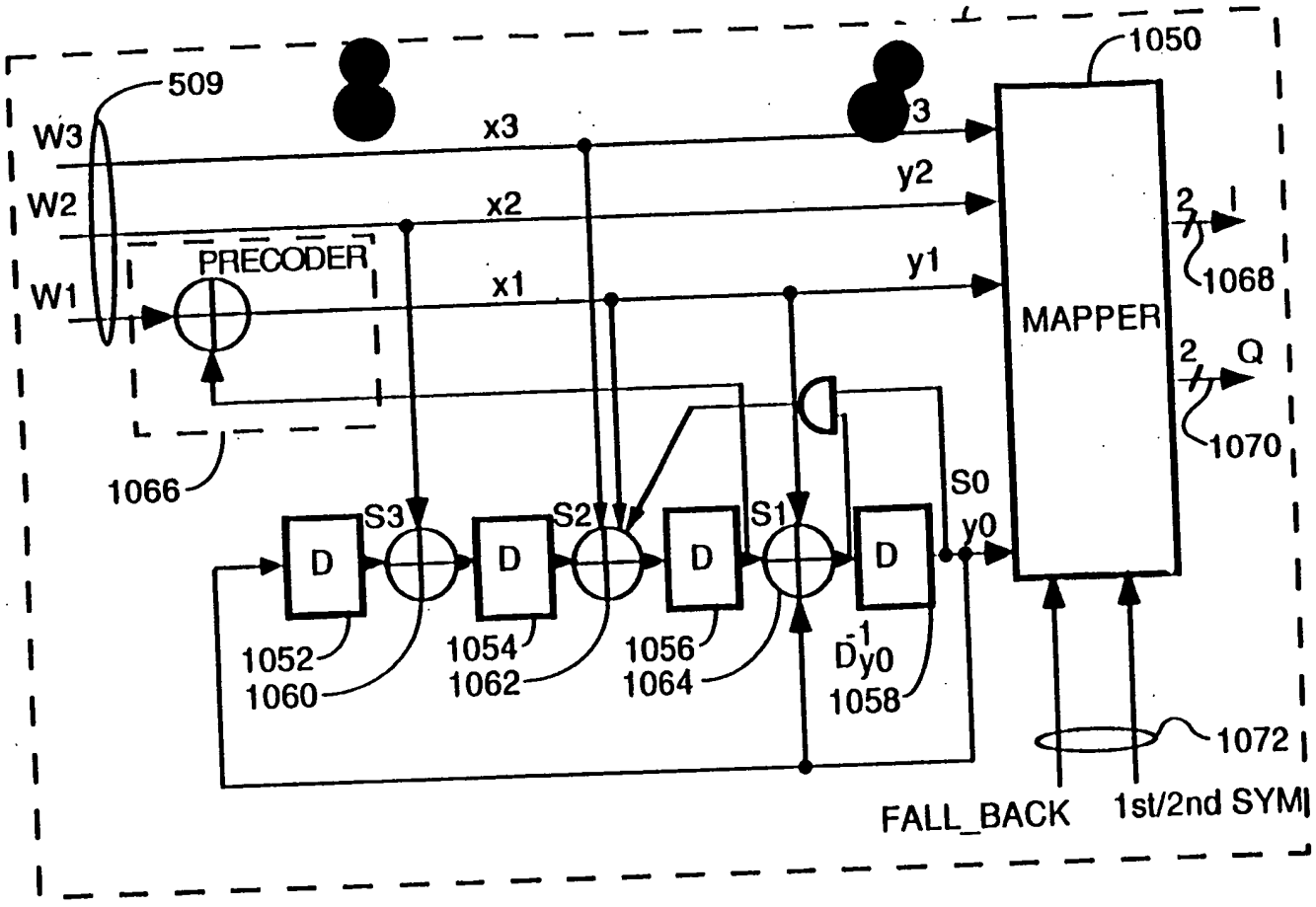

PAGE 1
MEMORY 300
144
ADDR
LOCATIONS
SYMBOL 3
SYMBOL 2
SYMBOL 1
TB1
TB2
TB3
TIME SLOT 1 /
CHANNEL
1 = 9 BITS
3 BITS
3 BITS
3 BITS

FIG. 20



PREFERRED TRELLIS ENCODER

FIG. 42

17

MAPPING FOR FALL-BACK MODE - LSB'S

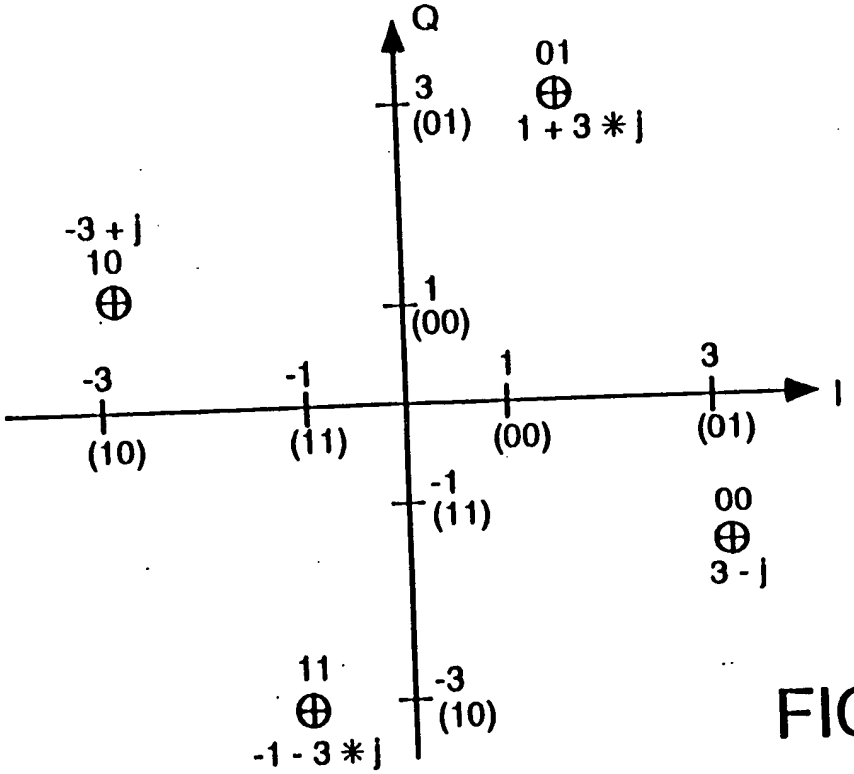
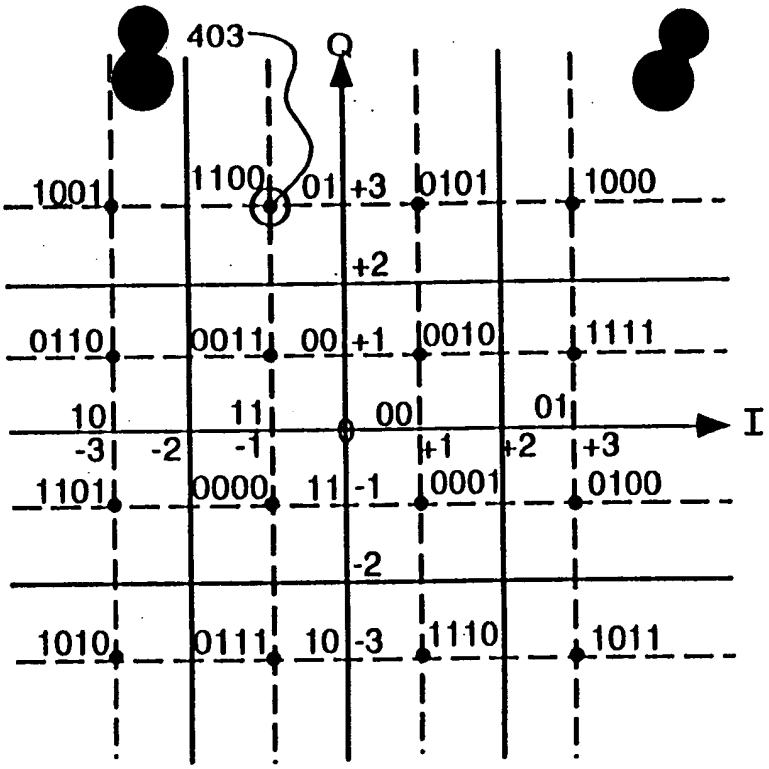


FIG. 43

21



18

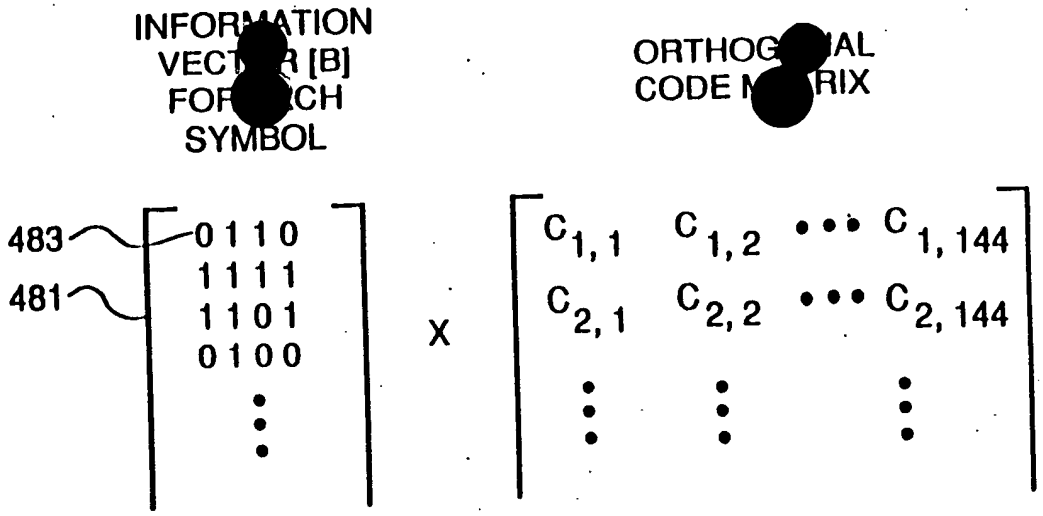
FIG. 21

CODE	INPHASE	QUADRATURE	
0000	111	111	= -1 - j
0001	001	111	= 1 - j
0010	001	001	= 1+ j
0011	111	001	= -1+ j
0100	011	111	= 3 - j
0101	001	011	= 1+ 3* j
0110	101	001	= -3 + j
0111	111	101	= -1 - 3* j
1000	011	011	=+3 + 3* j
1001	101	011	= -3 + 3* j
1010	101	101	= -3 - 3* j
1011	011	101	= 3 - 3* j
1100	111	011	= -1+ 3* j
1101	101	111	= -3 - j
1110	001	101	= 1 - 3* j
1111	011	001	= 3 + j

403

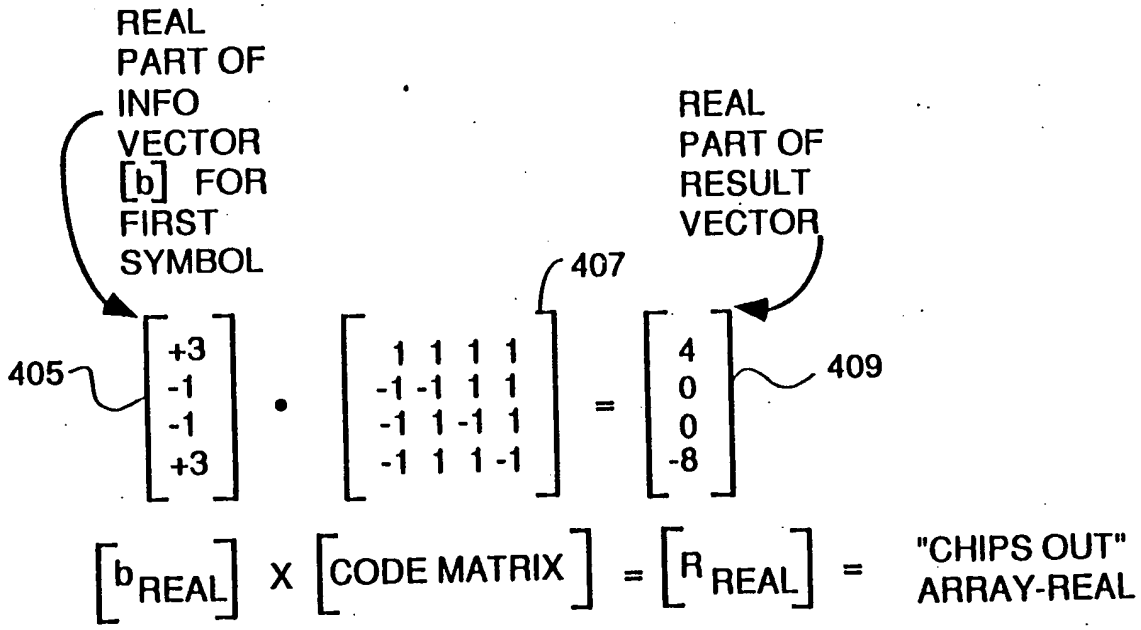
19

FIG. 22



20A

FIG. ~~23~~A



20B

FIG. ~~23~~B

LSBs y1 y0	PHASE	1+jQ
00	0	3-j
01	90	1+j3
10	180	-3+j
11	-90	-1-j3

MSBs y3 y2	PHASE difference (2nd-1st symbol)	1+jQ WHEN LSB=00	1+jQ WHEN LSB=01	1+jQ WHEN LSB=10	1+jQ WHEN LSB=11
00	0	3-j	1+j3	-3+j	-1-j3
01	90	1+j3	-3+j	-1-j3	3-j
10	180	-3+j	-1-j3	3-j	1+j3
11	-90	-1-j3	3-j	1+j3	-3+j

LSB & MSB FALLBACK MODE MAPPINGS

FIG. ~~4~~ 22

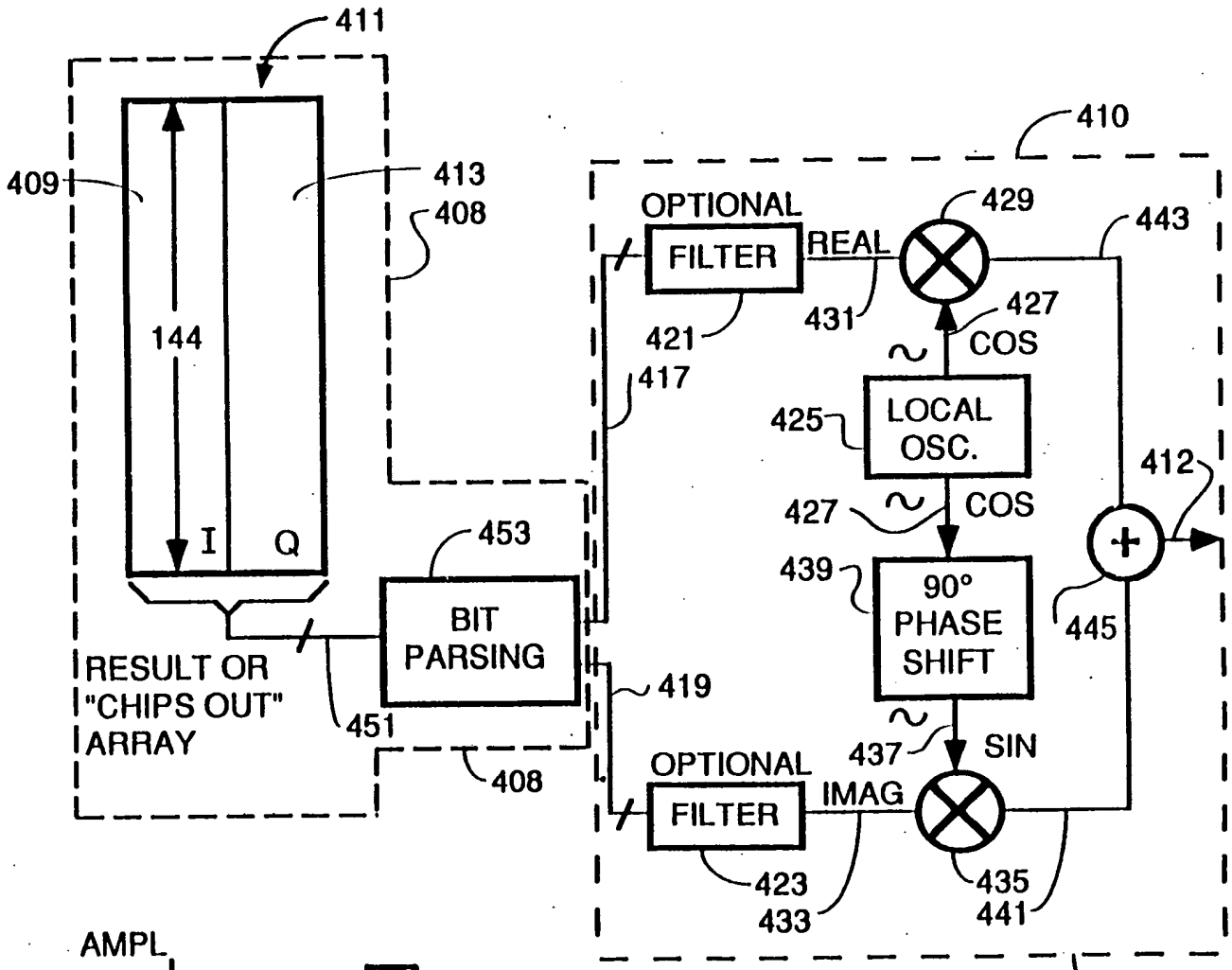

411
409
413
408
144
I
Q
453
BIT PARSING
RESULT OR "CHIPS OUT" ARRAY
451
408
410
OPTIONAL
FILTER
REAL
421
429
431
443
427
COS
417
425
LOCAL OSC.
427
COS
412
439
90° PHASE SHIFT
445
419
437
SIN
OPTIONAL
FILTER
IMAG
423
433
435
441
410

FIG. 24

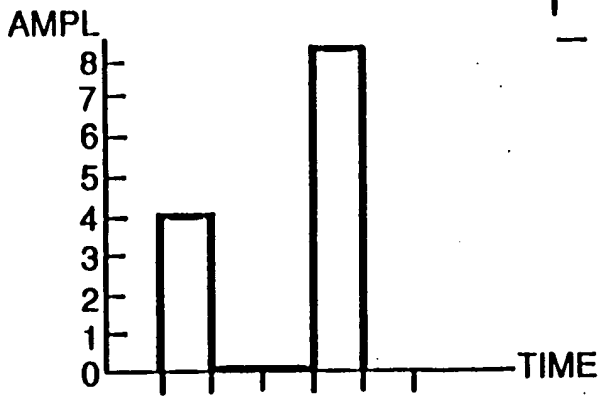
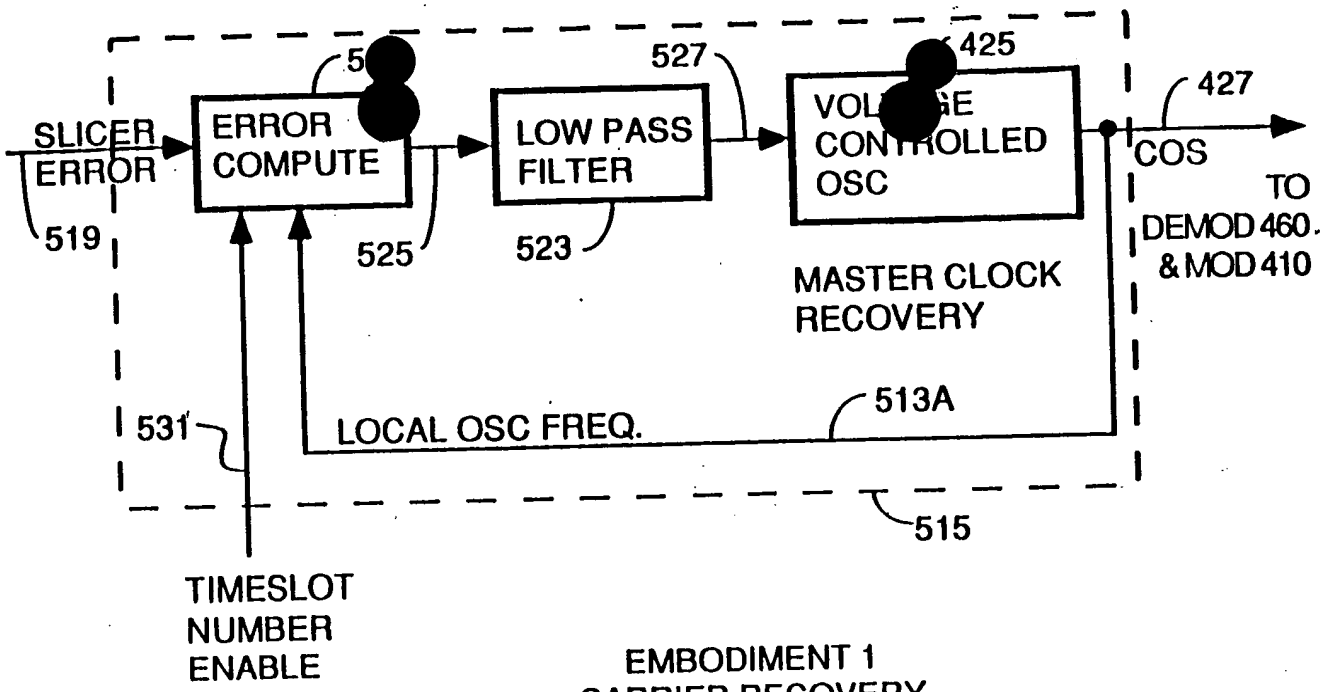

AMPL
8
7
6
5
4
3
2
1
0
TIME

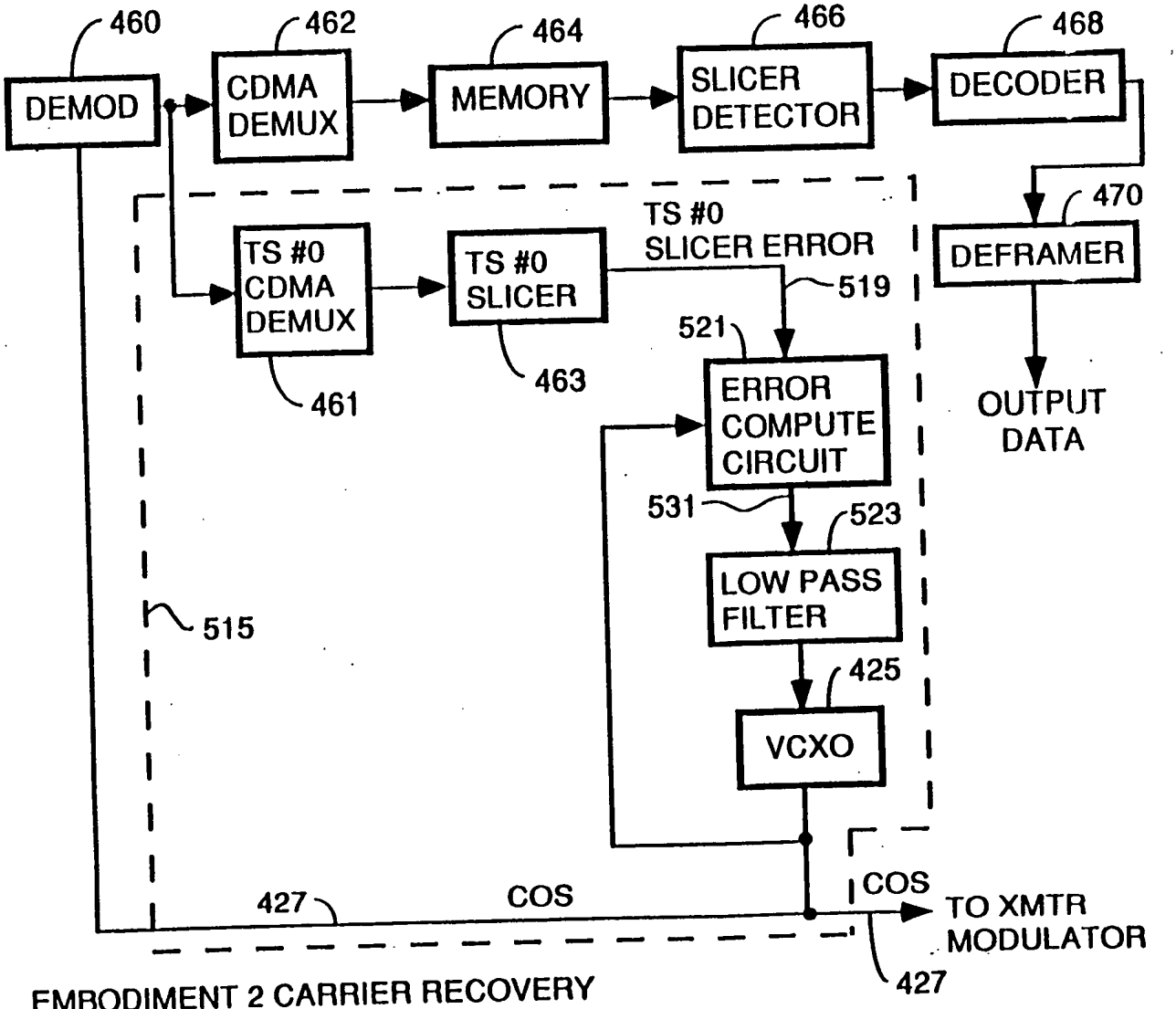
FIG. 25



EMBODIMENT 1
CARRIER RECOVERY

FIG. 35

25



EMBODIMENT 2 CARRIER RECOVERY

FIG. 36

26

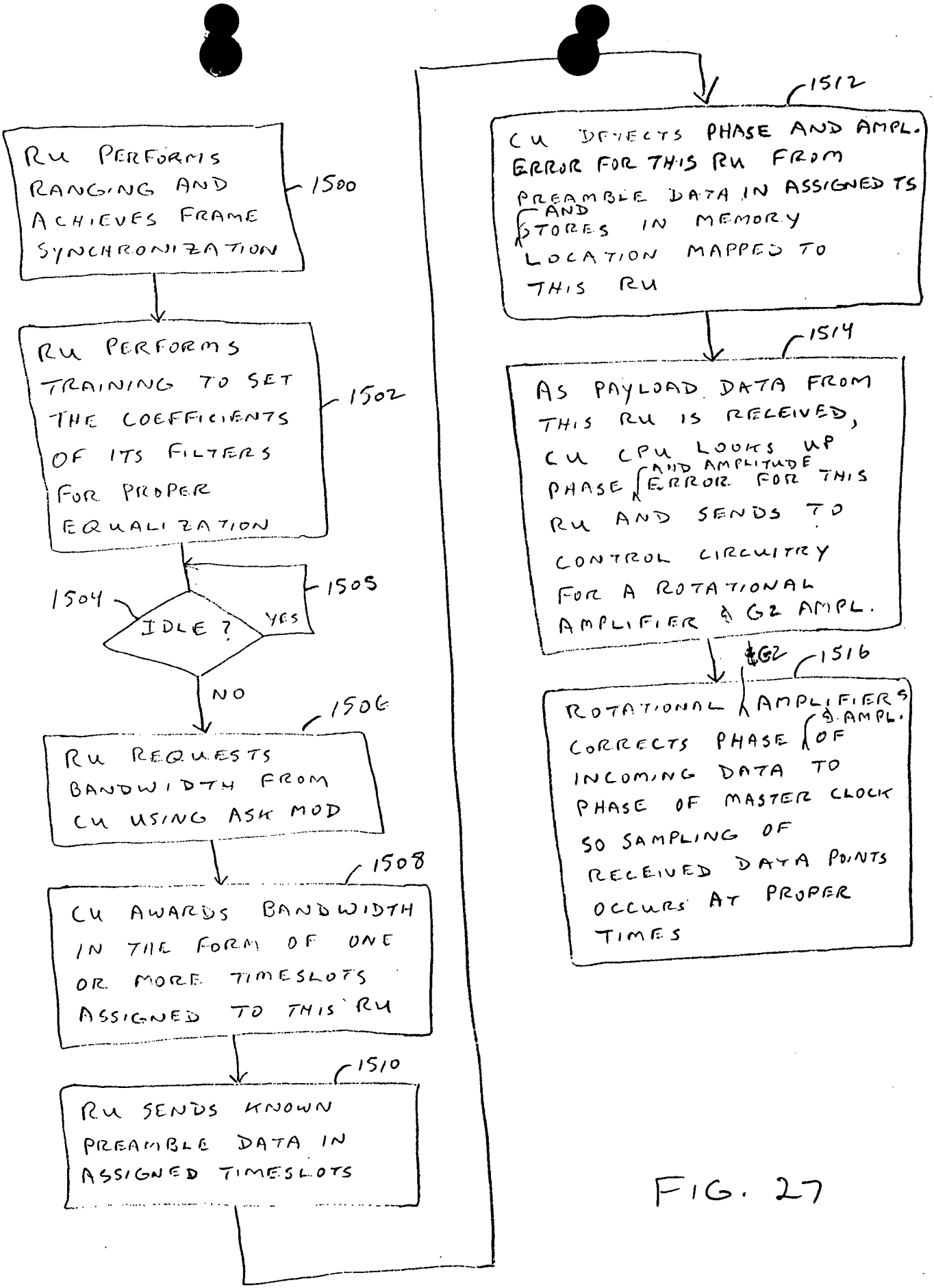
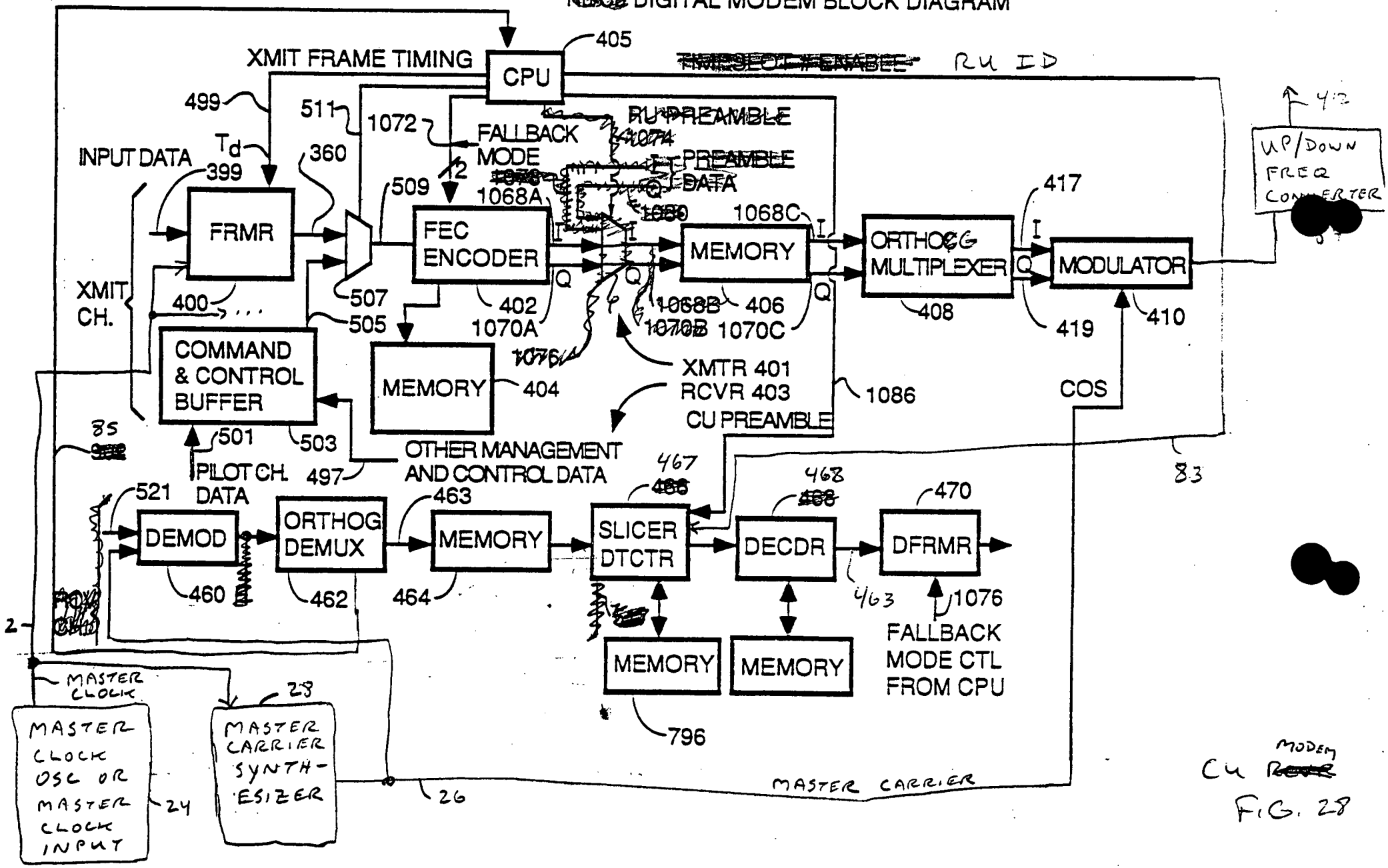

RU PERFORMS RANGING AND ACHIEVES FRAME SYNCHRONIZATION
1500
RU PERFORMS TRAINING TO SET THE COEFFICIENTS OF ITS FILTERS FOR PROPER EQUALIZATION
1502
1504
IDLE ?
YES
1505
NO
RU REQUESTS BANDWIDTH FROM CU USING ASK MOD
1506
CU AWARDS BANDWIDTH IN THE FORM OF ONE OR MORE TIMESLOTS ASSIGNED TO THIS RU
1508
RU SENDS KNOWN PREAMBLE DATA IN ASSIGNED TIMESLOTS
1510
CU DETECTS PHASE AND AMPL. ERROR FOR THIS RU FROM PREAMBLE DATA IN ASSIGNED TS AND STORES IN MEMORY LOCATION MAPPED TO THIS RU
1512
AS PAYLOAD DATA FROM THIS RU IS RECEIVED, CU CPU LOOKS UP PHASE AND AMPLITUDE ERROR FOR THIS RU AND SENDS TO CONTROL CIRCUITRY FOR A ROTATIONAL AMPLIFIER & G2 AMPL.
1514
G2
ROTATIONAL AMPLIFIERS CORRECTS PHASE & AMPL. OF INCOMING DATA TO PHASE OF MASTER CLOCK SO SAMPLING OF RECEIVED DATA POINTS OCCURS AT PROPER TIMES
1516

FIG. 27


DIGITAL MODEM BLOCK DIAGRAM
XMIT FRAME TIMING
CPU
405
RU ID
499
511
1072
FALLBACK MODE
RU PREAMBLE
PREAMBLE
DATA
INPUT DATA
Td
360
399
FRMR
509
1068A
FEC ENCODER
1068C
MEMORY
ORTHOG MULTIPLEXER
MODULATOR
417
UP/DOWN FREQ CONVERTER
XMIT CH.
400
507
505
402
1070A
1068B
406
1070C
408
419
410
COMMAND & CONTROL BUFFER
MEMORY
404
XMTR 401
RCVR 403
CU PREAMBLE
1086
COS
85
501
503
PILOT CH. DATA
497
OTHER MANAGEMENT AND CONTROL DATA
83
521
DEMOD
460
ORTHOG DEMUX
462
463
MEMORY
464
467
SLICER DTCTR
468
DECDR
470
DFRMR
463
1076
FALLBACK MODE CTL FROM CPU
MEMORY
MEMORY
796
MASTER CLOCK
MASTER CLOCK OSC OR MASTER CLOCK INPUT
24
29
MASTER CARRIER SYNTHESIZER
26
MASTER CARRIER
MODEM CU
FIG. 28

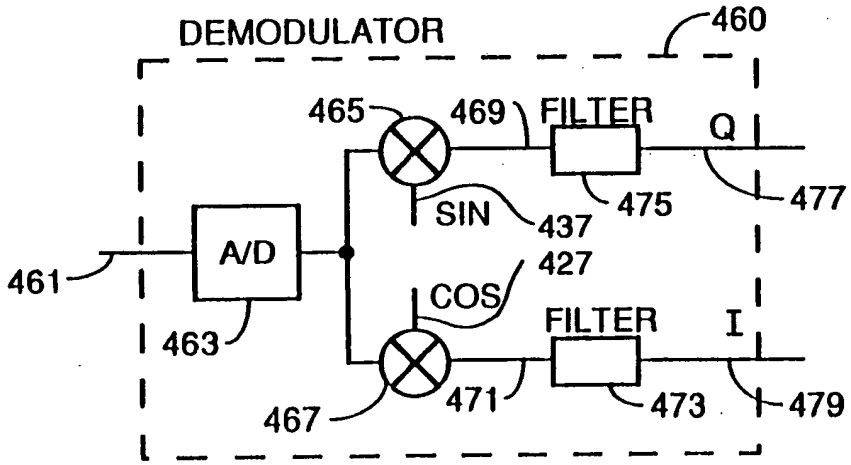
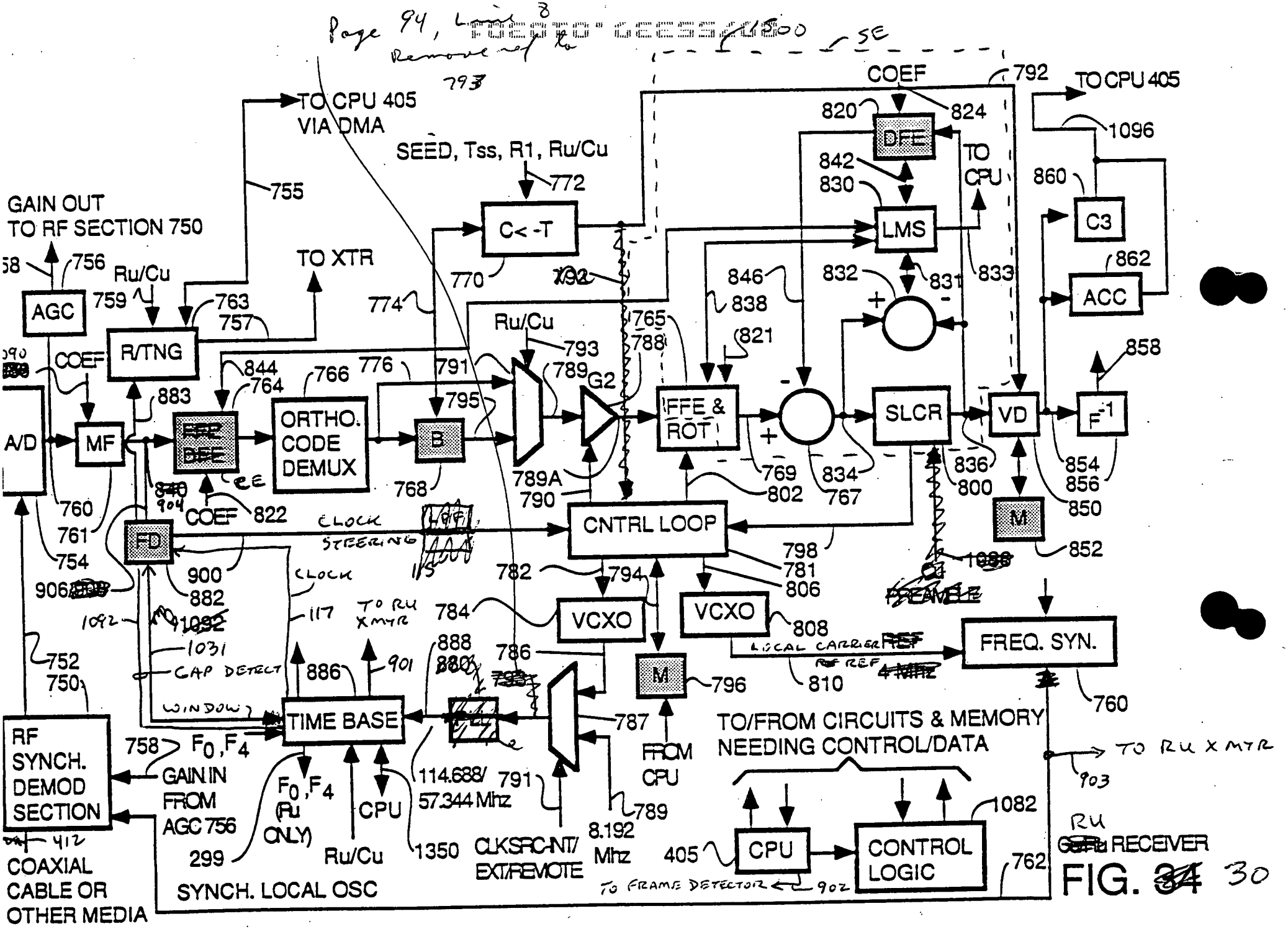

DEMODULATOR
460
465
469
FILTER
Q
475
477
SIN
437
461
A/D
427
COS
FILTER
I
463
467
471
473
479

FIG. 26

29


TO CPU 405
VIA DMA
SEED, Tss, R1, Ru/Cu
772
755
GAIN OUT
TO RF SECTION 750
TO XTR
AGC
R/TNG
Ru/Cu
759
763
757
756
COEF
844
764
883
766
776
791
774
770
C<-T
Ru/Cu
793
789
G2
795
765
788
789A
790
768
ORTHO.
CODE
DEMUX
B
A/D
MF
FFE
DFE
760
761
754
906
904
822
840
FD
CLOCK
STEERING
900
882
CLOCK
117
TO RU
XMTR
1092
1031
CAP DETECT
WINDOW
752
750
RF
SYNCH.
DEMOD
SECTION
758
F0, F4
GAIN IN
FROM
AGC 756
412
COAXIAL
CABLE OR
OTHER MEDIA
299
F0, F4
(Ru
ONLY)
886
901
888
786
TIME BASE
CPU
Ru/Cu
1350
SYNCH. LOCAL OSC
114.688/
57.344 Mhz
791
CLKSRC-INT/
EXT/REMOTE
787
789
8.192
Mhz
CNTRL LOOP
782
794
798
781
806
VCXO
784
VCXO
808
M
796
FROM
CPU
LOCAL CARRIER REF
RF REF
4 Mhz
810
FREQ. SYN.
760
TO/FROM CIRCUITS & MEMORY
NEEDING CONTROL/DATA
405
CPU
CONTROL
LOGIC
1082
762
TO FRAME DETECTOR
902
TO RU XMTR
903
RU
RECEIVER
COEF
792
TO CPU 405
1096
820
824
DFE
842
830
TO
CPU
LMS
860
C3
862
ACC
846
838
832
831
833
821
858
IFFE &
ROT
SLCR
VD
F-1
769
834
767
836
800
802
854
856
850
M
852
FIG. 30

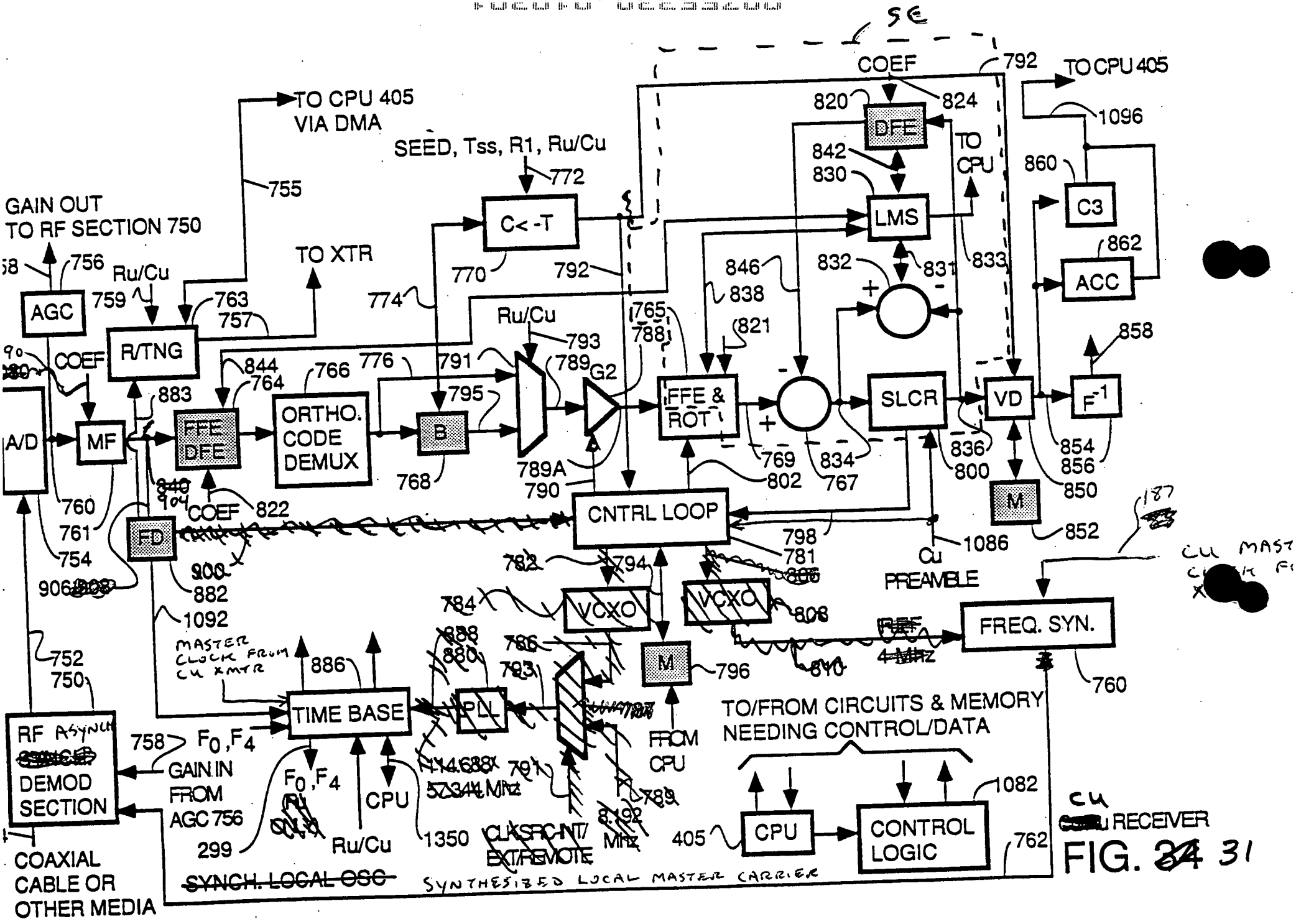

TO CPU 405
VIA DMA
SEED, Tss, R1, Ru/Cu
772
755
GAIN OUT
TO RF SECTION 750
TO XTR
C<-T
770
792
774
COEF
792
TO CPU 405
820
824
DFE
1096
842
830
TO
CPU
LMS
860
C3
862
ACC
846
838
832
831
833
765
788
821
858
AGC
759
Ru/Cu
763
757
R/TNG
Ru/Cu
793
776
791
789
G2
766
764
844
883
795
768
789A
790
FFE &
ROT
769
834
767
802
SLCR
VD
F-1
836
800
854
856
850
A/D
MF
FFE
DFE
ORTHO.
CODE
DEMUX
B
760
761
754
906
840
904
COEF
822
FD
CNTRL LOOP
798
781
1086
Cu
PREAMBLE
M
852
782
794
784
VCXO
VCXO
808
882
1092
752
750
MASTER
CLOCK FROM
CU XMTR
886
TIME BASE
PLL
786
793
M
796
FREQ. SYN.
760
TO/FROM CIRCUITS & MEMORY
NEEDING CONTROL/DATA
RF ASYNCH
DEMOD
SECTION
758
F_0, F_4
GAIN IN
FROM
AGC 756
299
F_0, F_4
Ru/Cu
CPU
1350
FROM
CPU
791
789
405
CPU
CONTROL
LOGIC
1082
762
CU RECEIVER
COAXIAL
CABLE OR
OTHER MEDIA
SYNCH. LOCAL OSC
SYNTHESIZED LOCAL MASTER CARRIER

FIG. 31

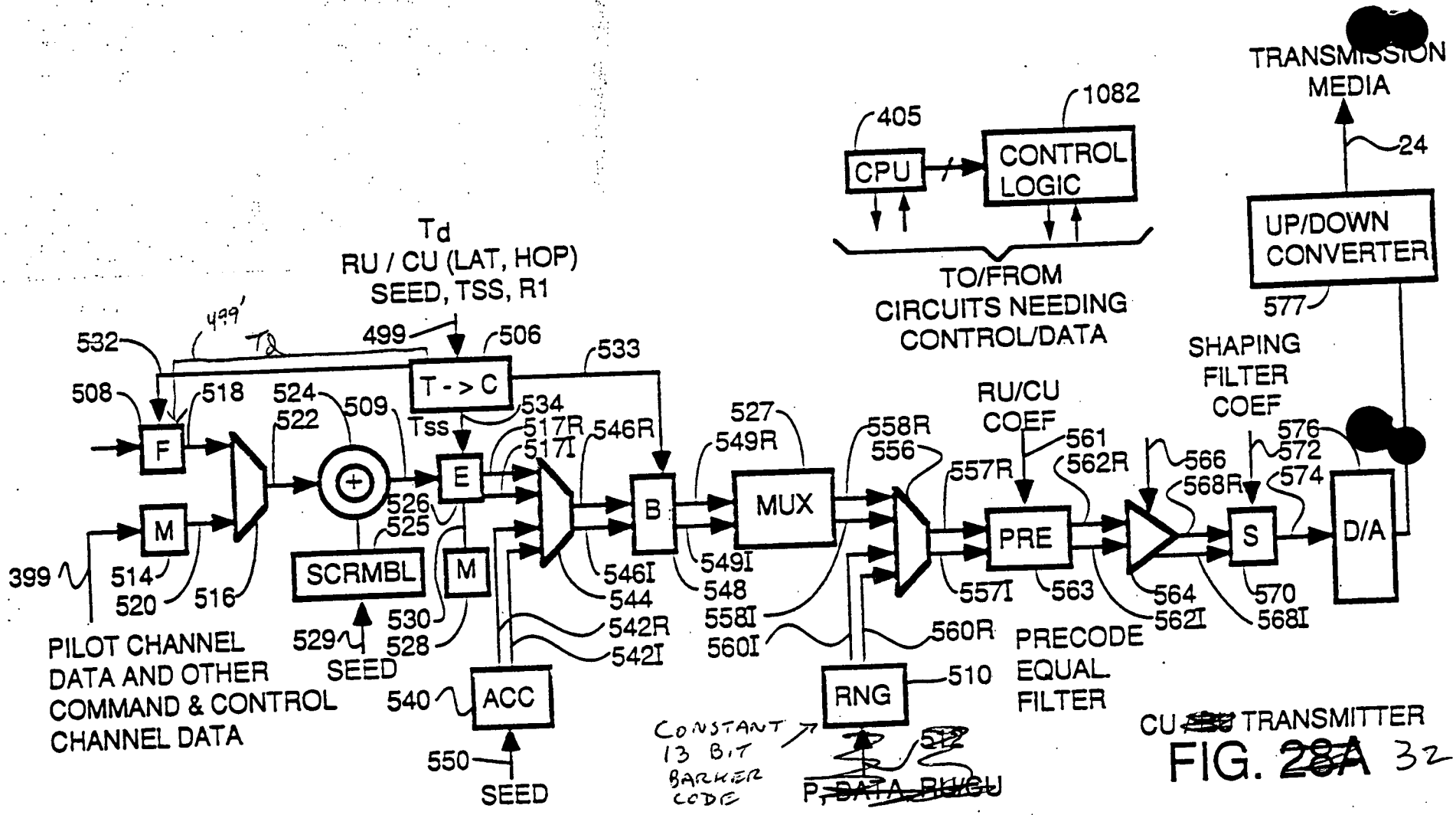


FIG. 28A

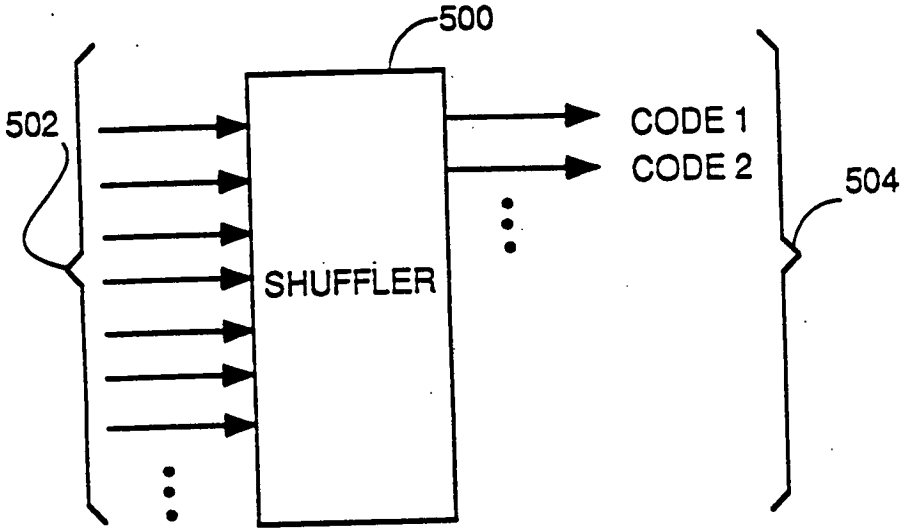


FIG. 27 38

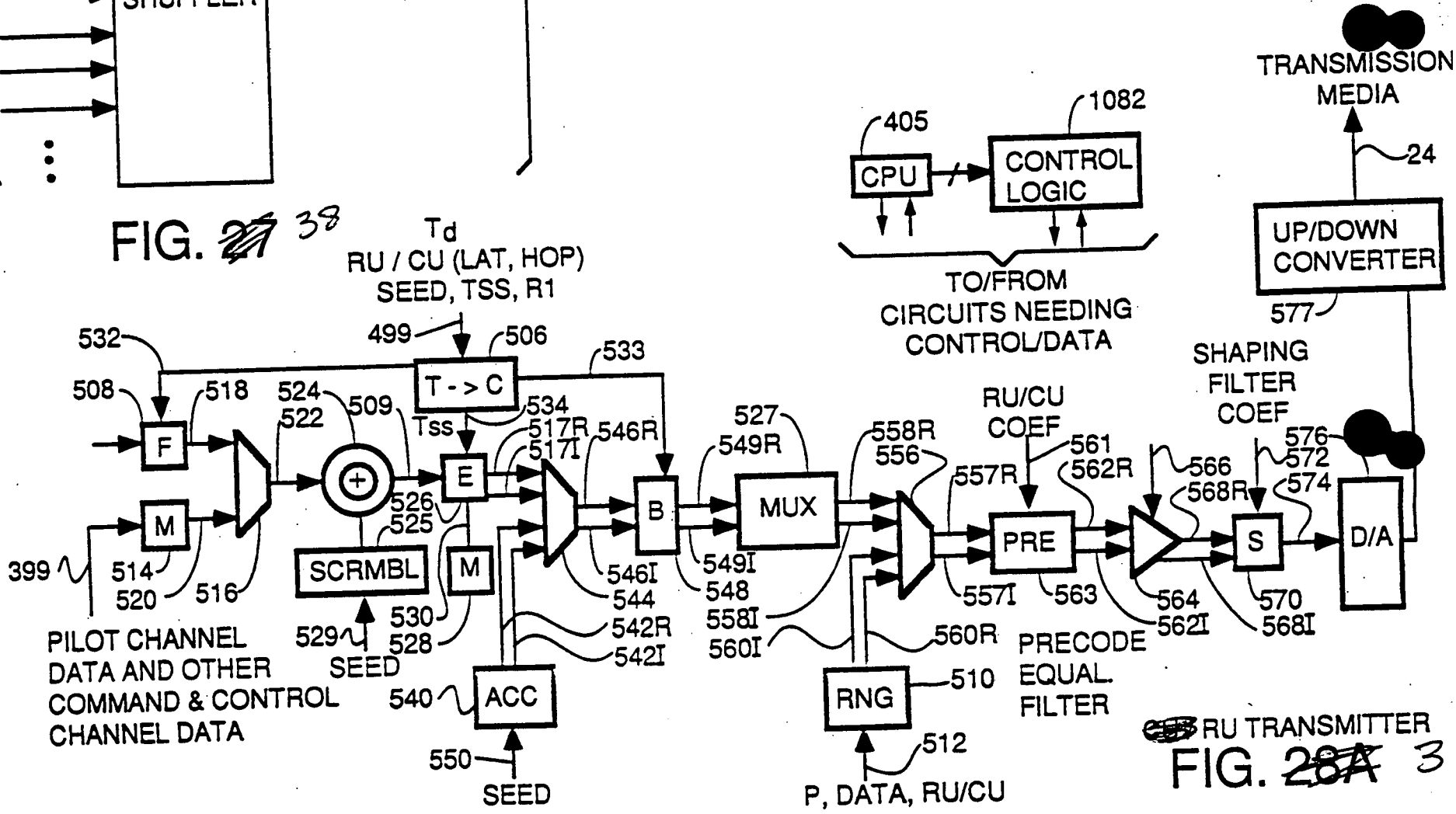
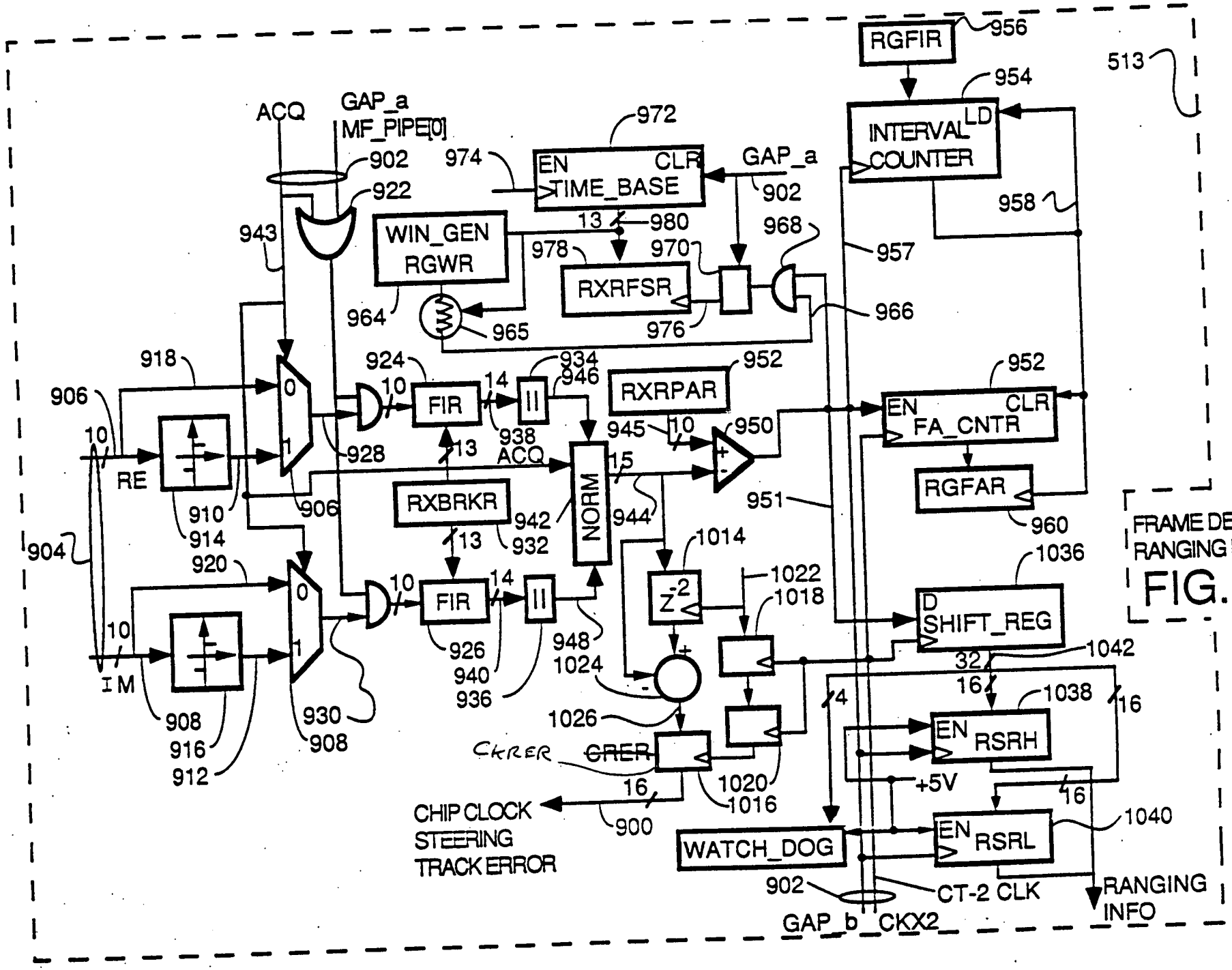


FIG. 28A 3



FRAME DETECTOR/
RANGING DETECTOR

FIG. 38

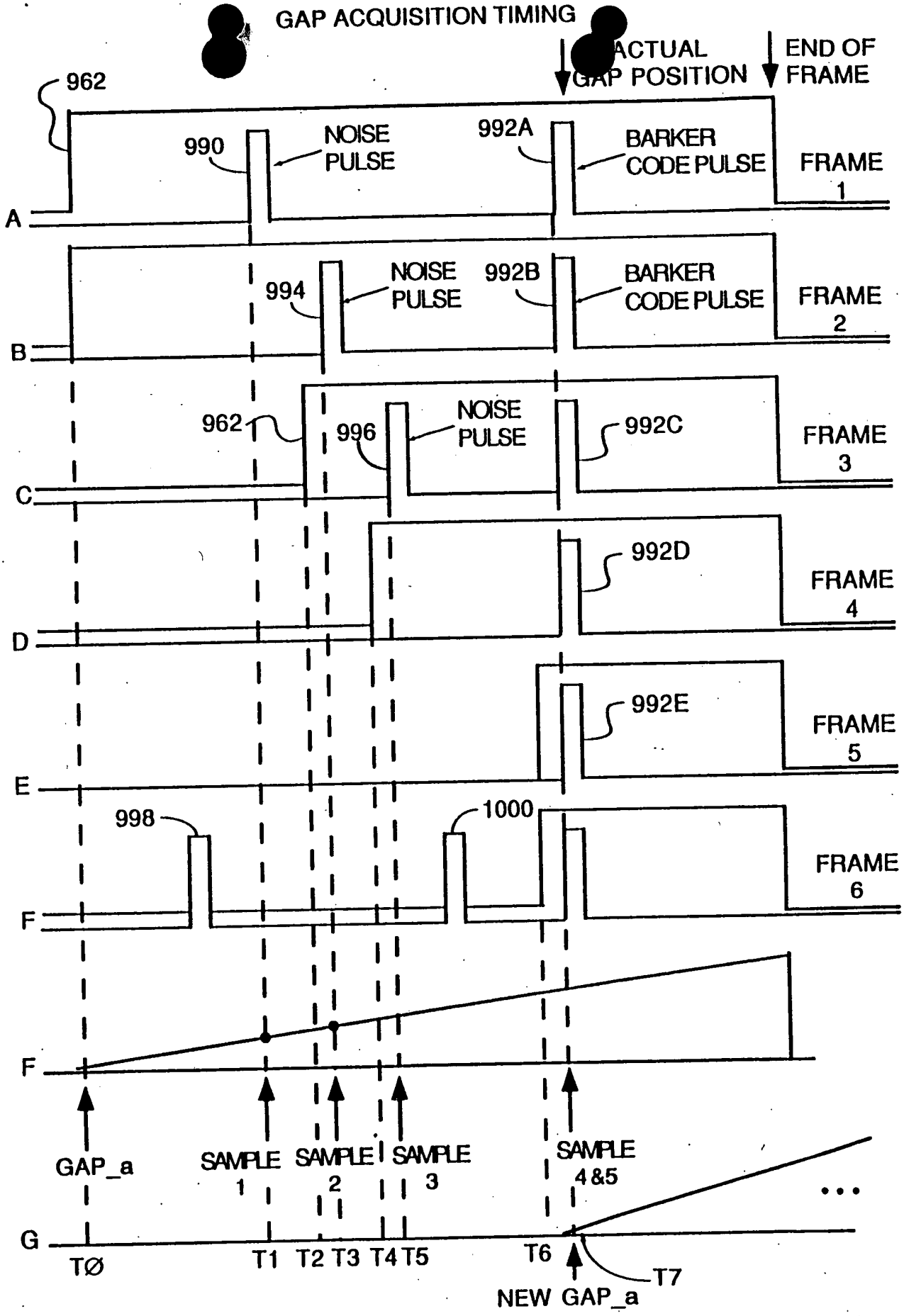
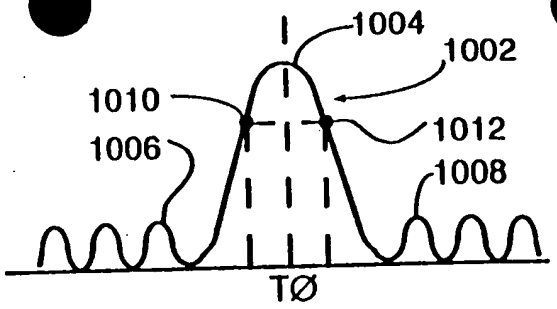
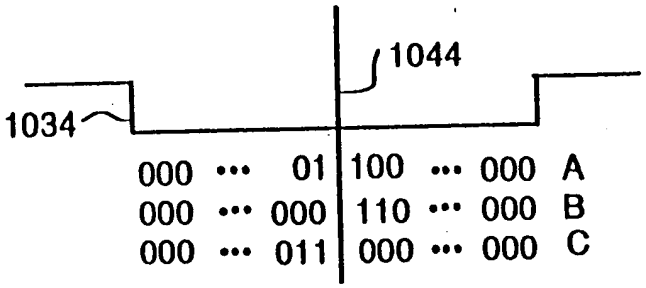

GAP ACQUISITION TIMING
ACTUAL GAP POSITION
END OF FRAME
962
990
NOISE PULSE
992A
BARKER CODE PULSE
FRAME 1
A
994
NOISE PULSE
992B
BARKER CODE PULSE
FRAME 2
B
962
996
NOISE PULSE
992C
FRAME 3
C
992D
FRAME 4
D
992E
FRAME 5
E
998
1000
FRAME 6
F
F
GAP_a
SAMPLE 1
SAMPLE 2
SAMPLE 3
SAMPLE 4&5
G
TØ
T1 T2 T3 T4 T5
T6
T7
NEW GAP_a

FIG. 39 35



36

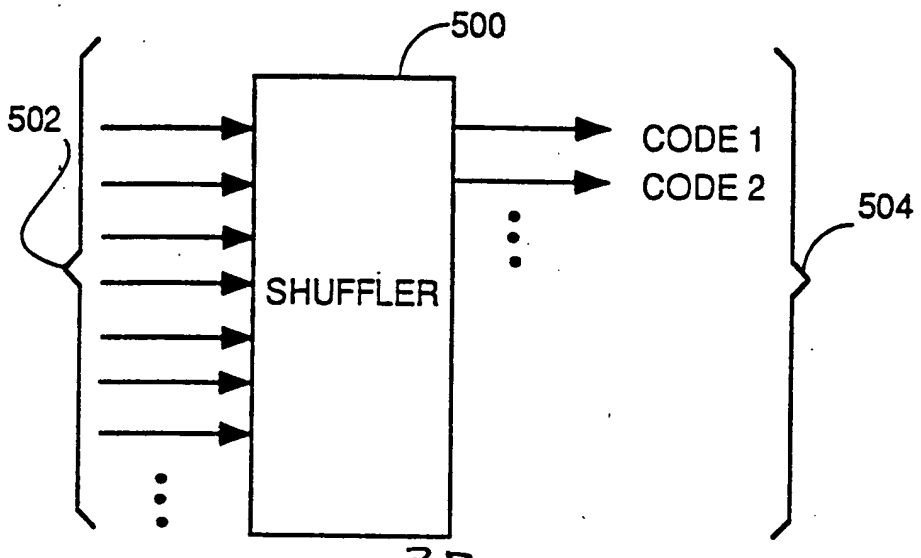
FIG. ~~40~~



37

FIG. ~~41~~

FINE TUNING TO CENTER BARRIER CODE



38

FIG. 27

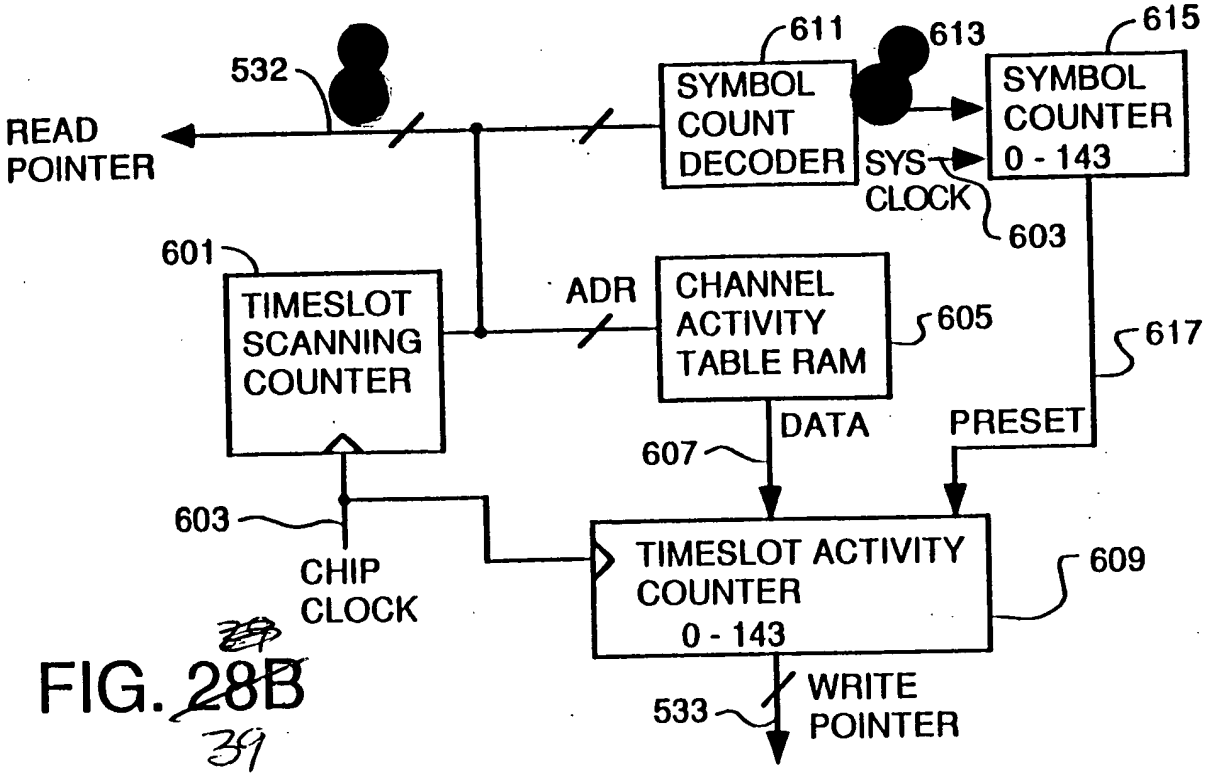


FIG. 28B

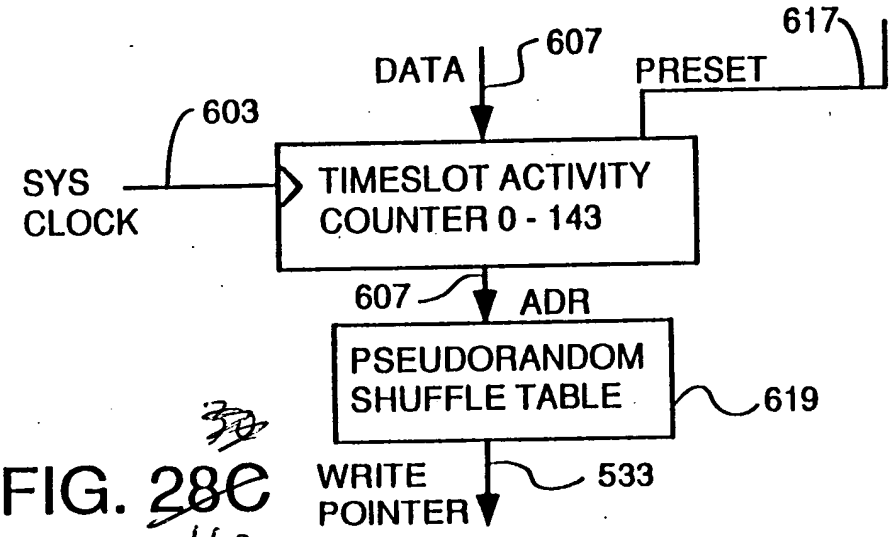


FIG. 28C

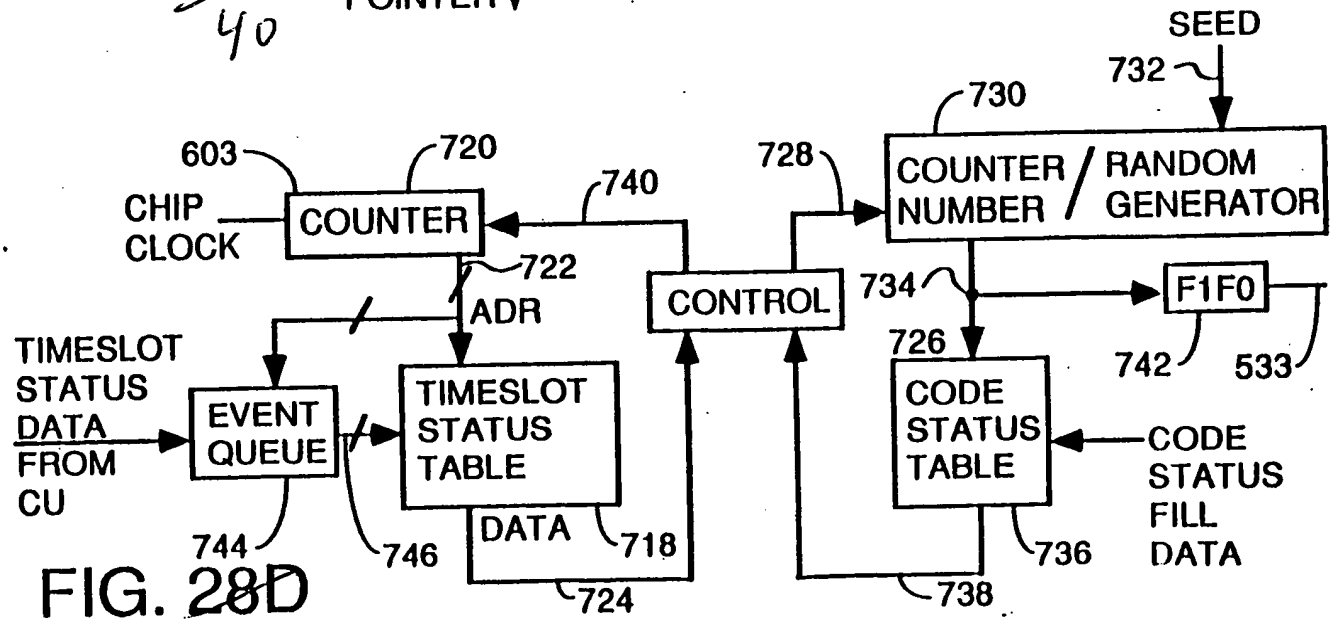
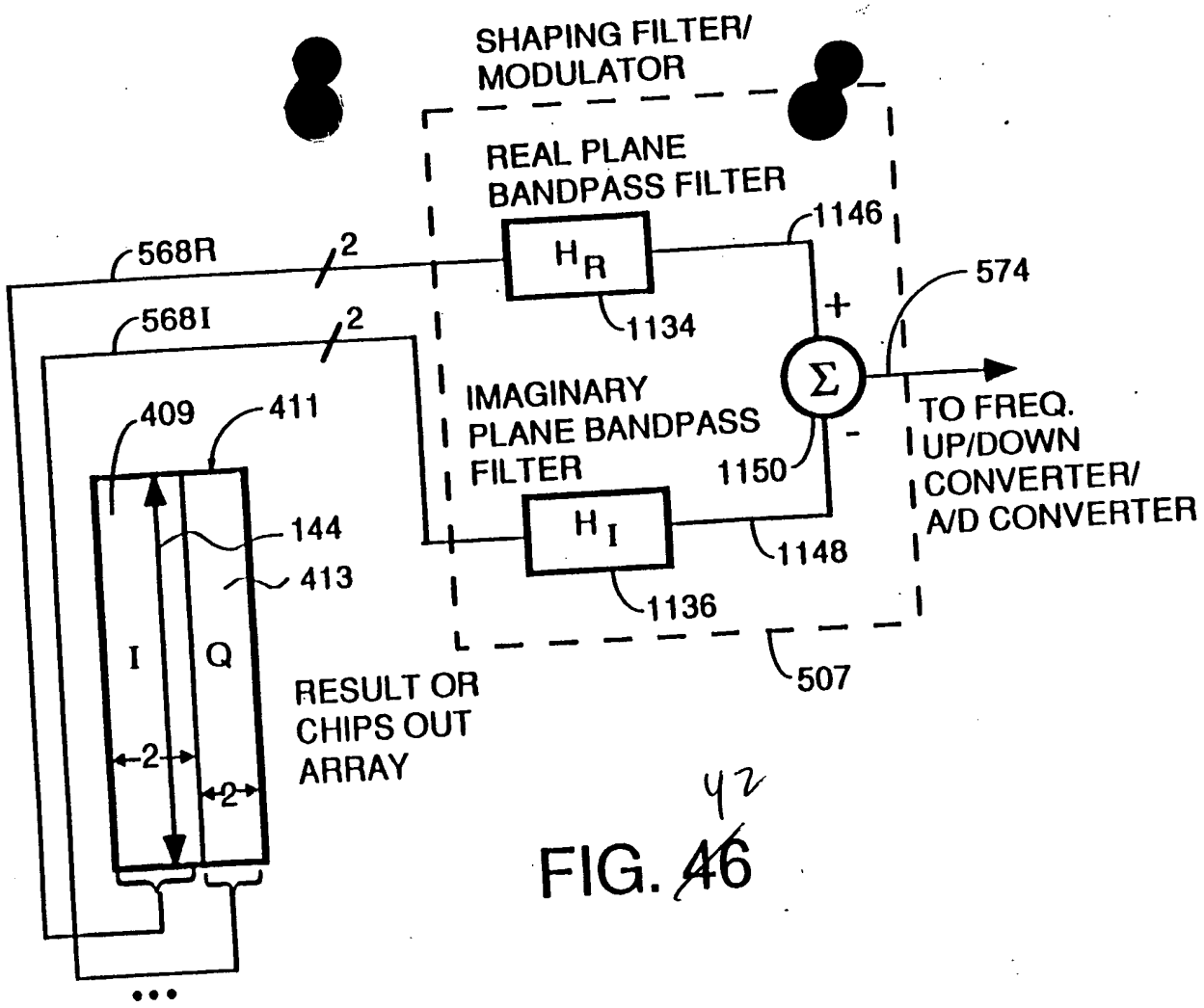
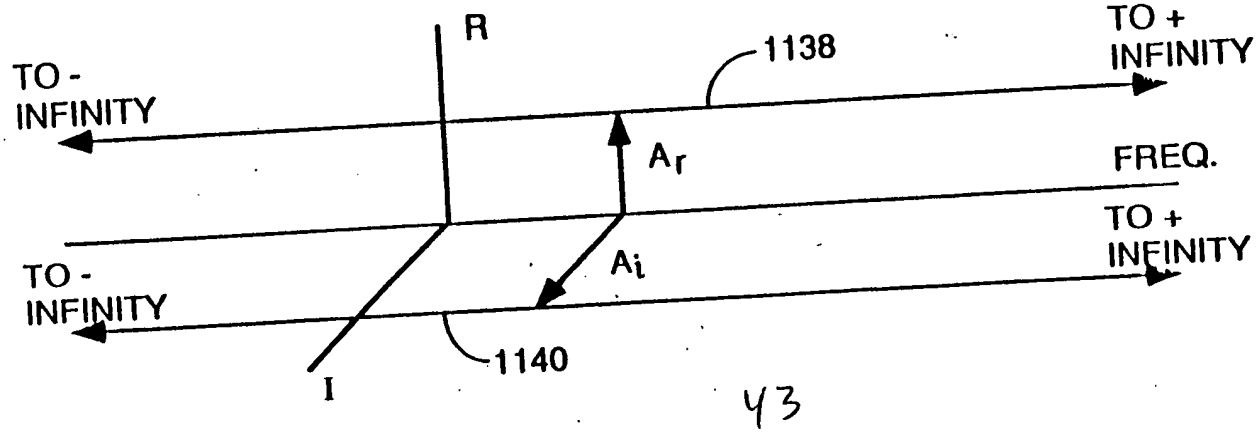


FIG. 28D



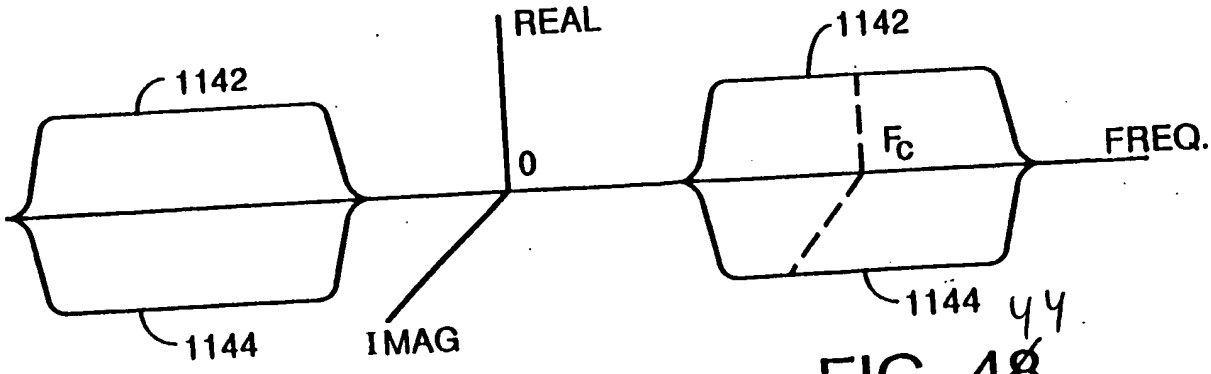
42

FIG. 46



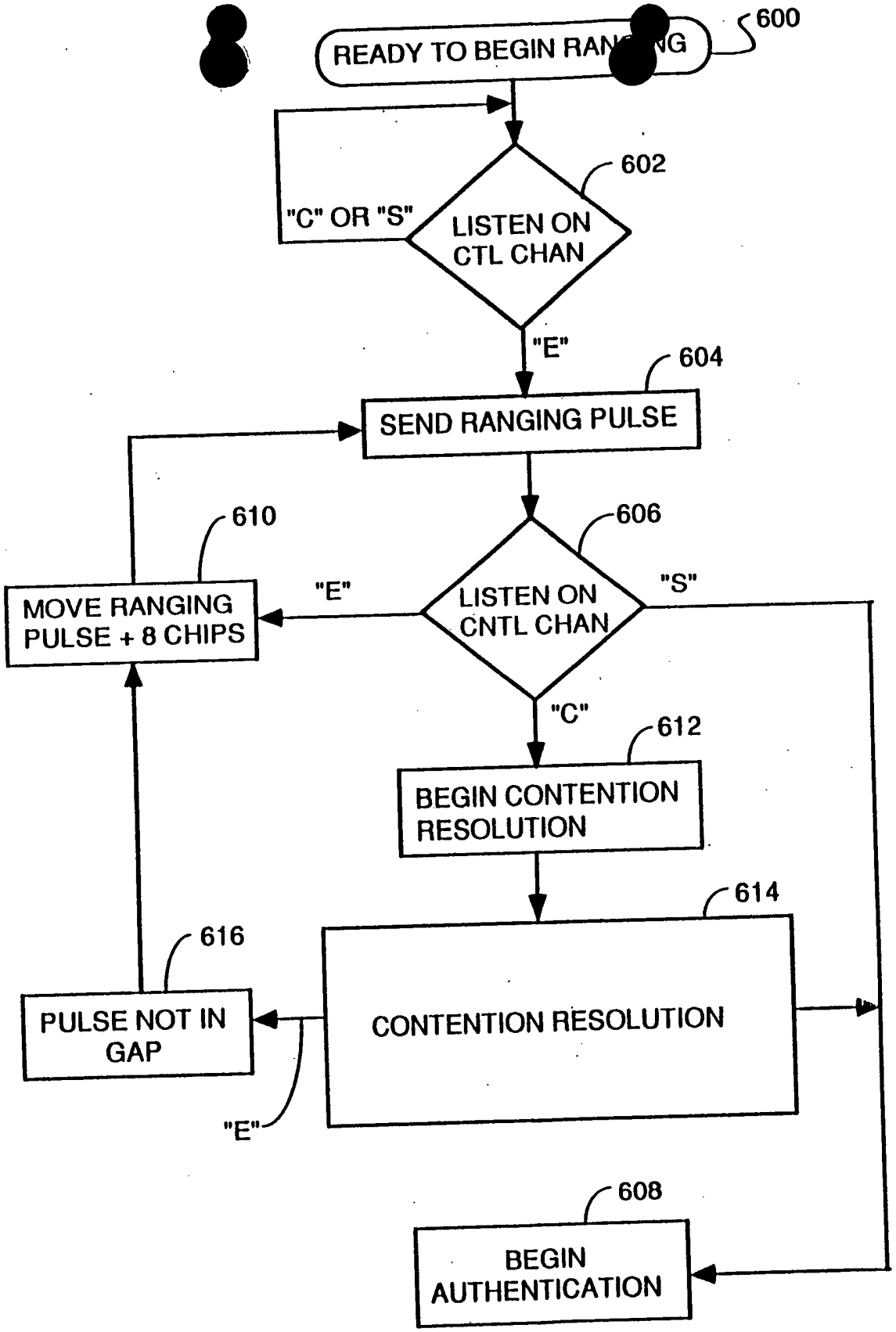
43

FIG. 47



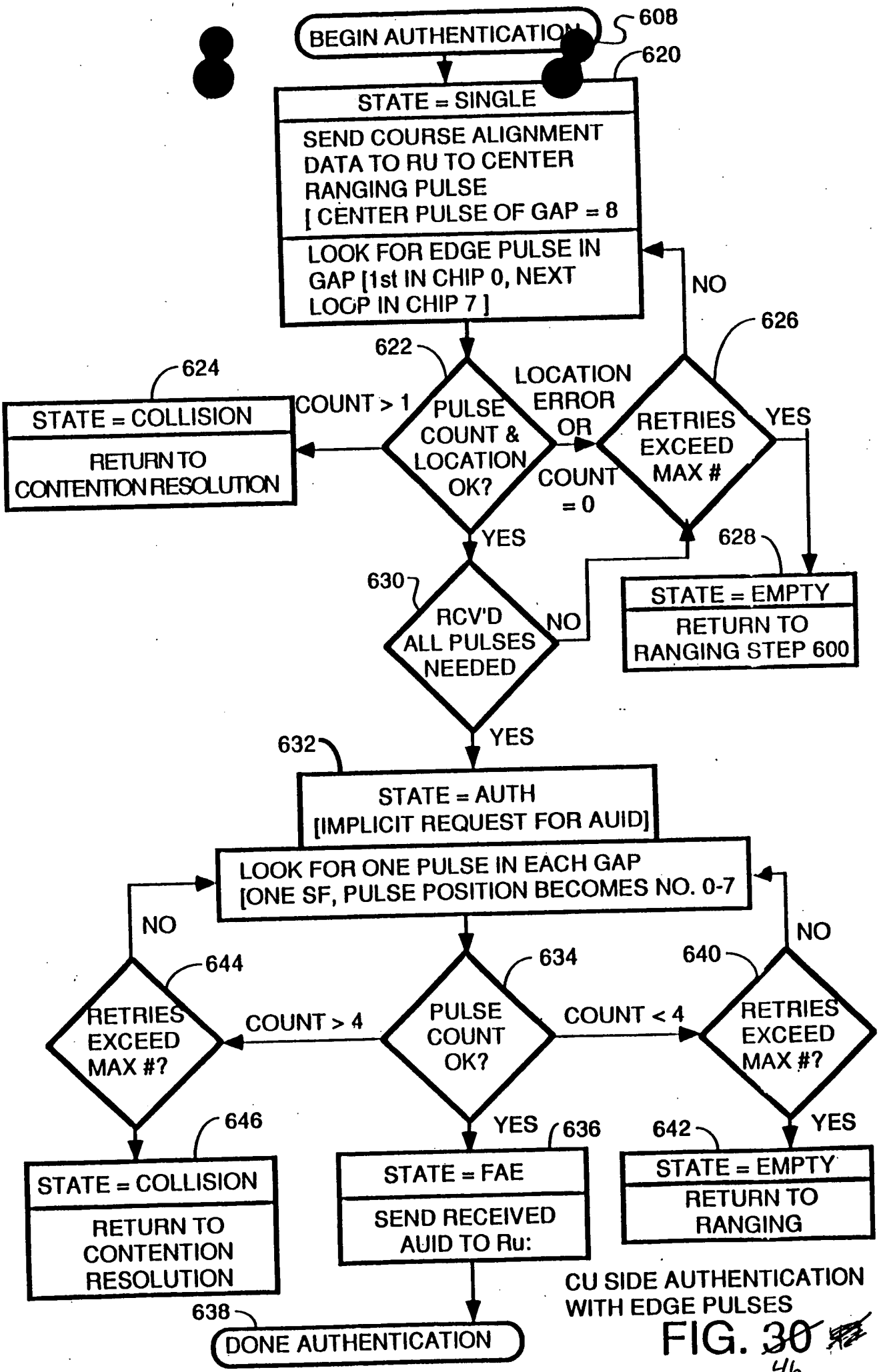
44

FIG. 48



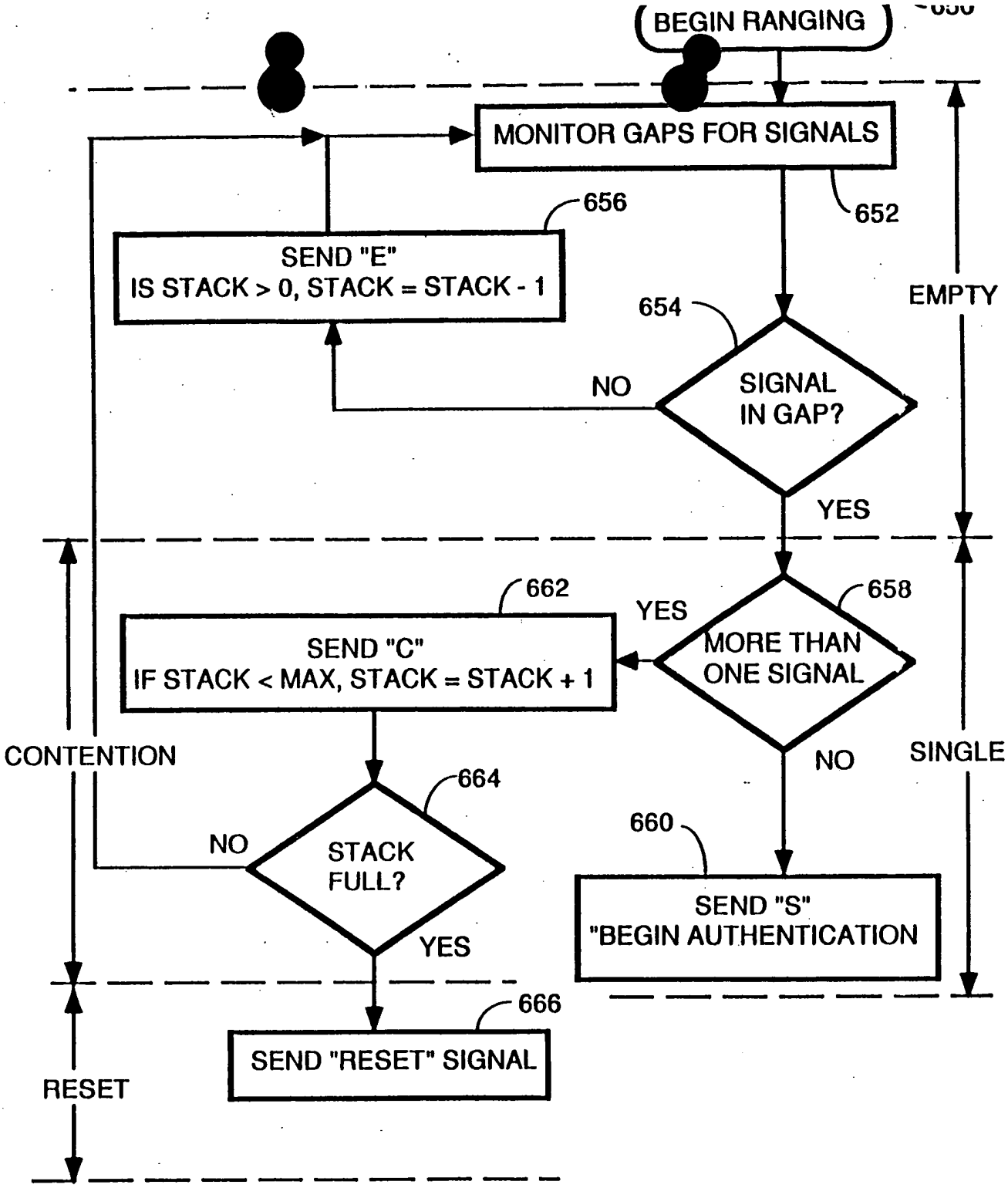
RU RANGING

FIG. 29



CU SIDE AUTHENTICATION WITH EDGE PULSES

FIG. 30

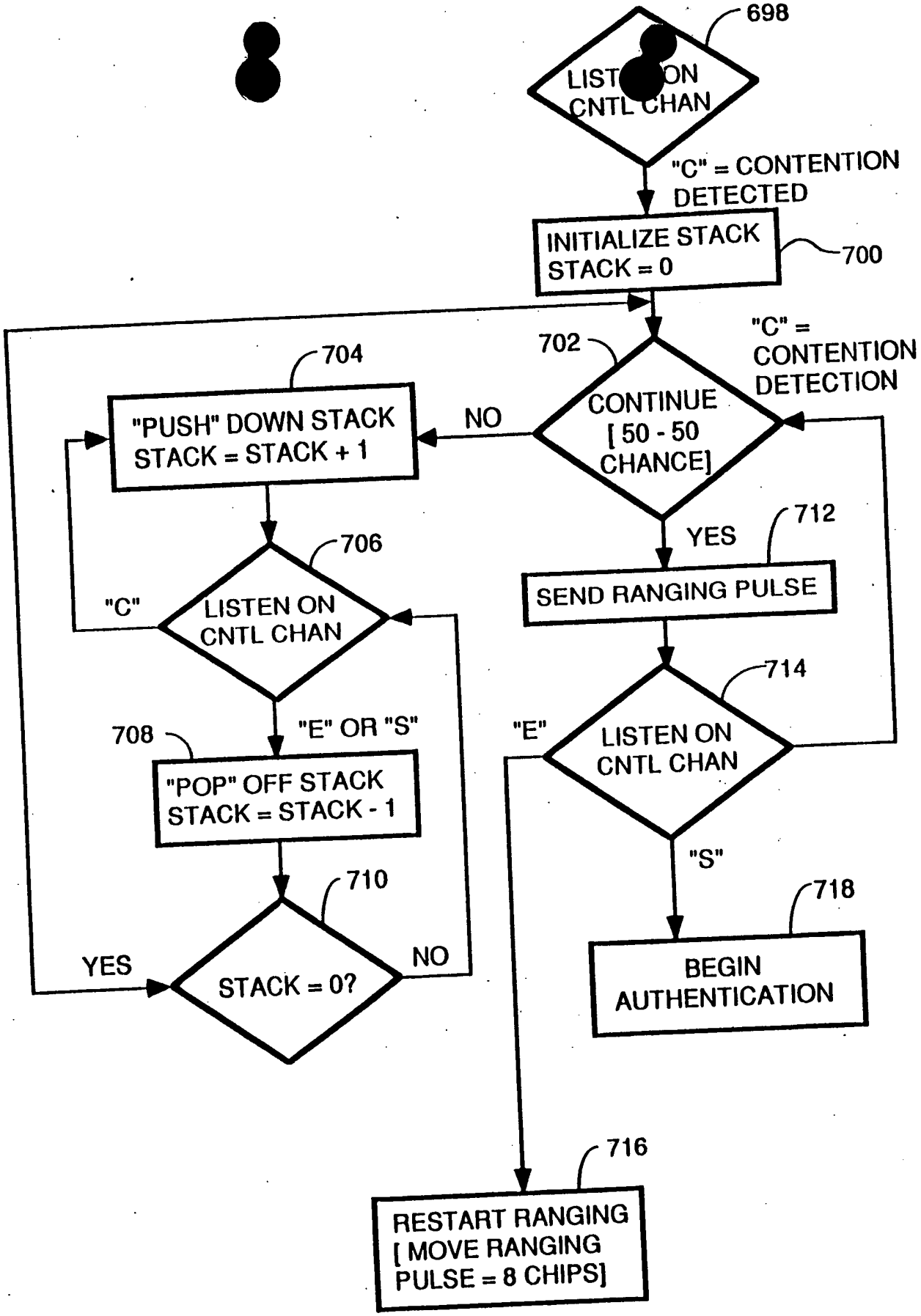


CU RANGING & CONTENTION RESOLUTION

~~RANGING AND CONTENTION RESOLUTION~~
~~CU SIDE~~

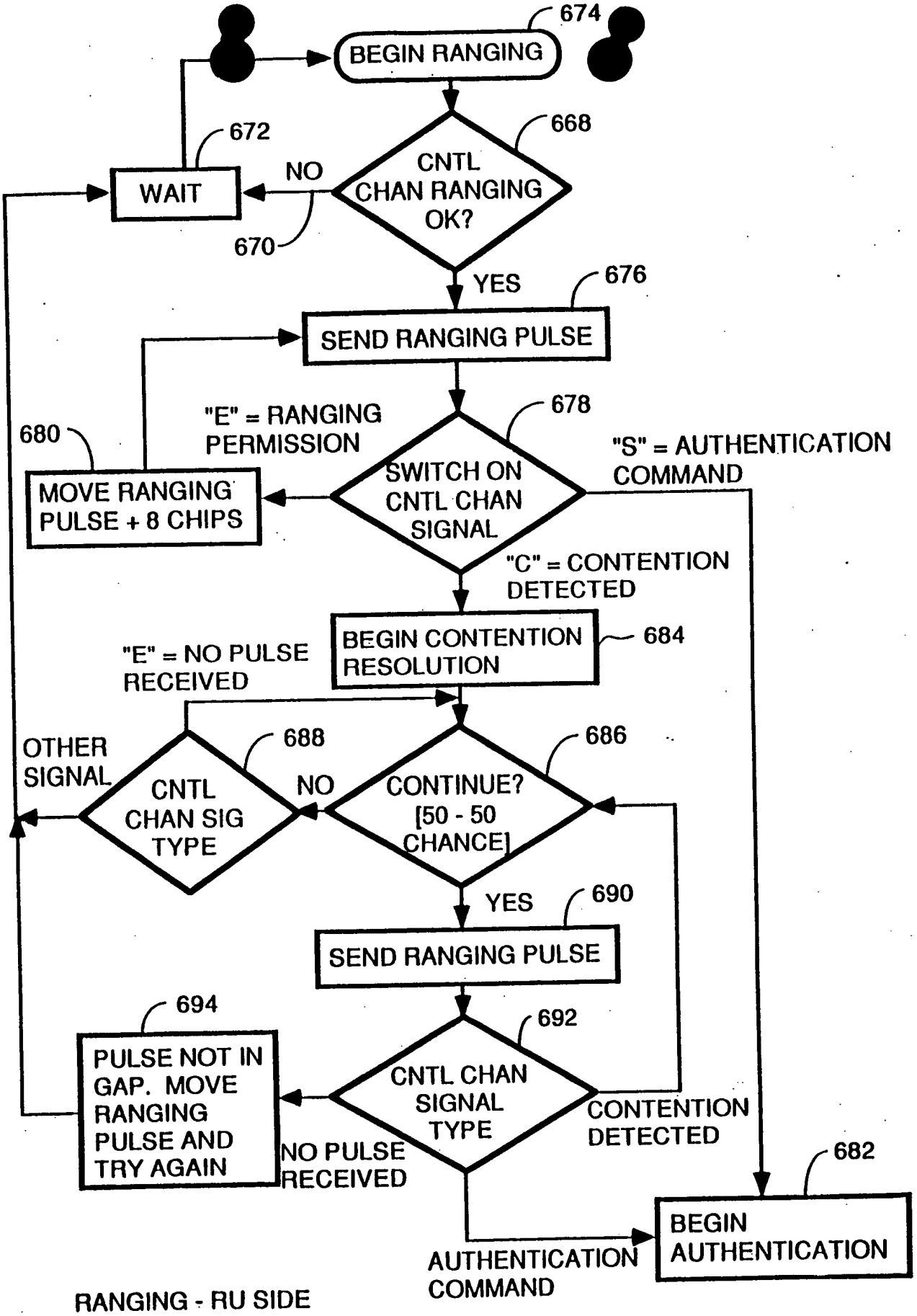
FIG. 31

47



CONTENTION RESOLUTION - RU USING BINARY STACK

FIG. 33



RANGING - RU SIDE BINARY TREE ALGORITHM

FIG. 32

50

49

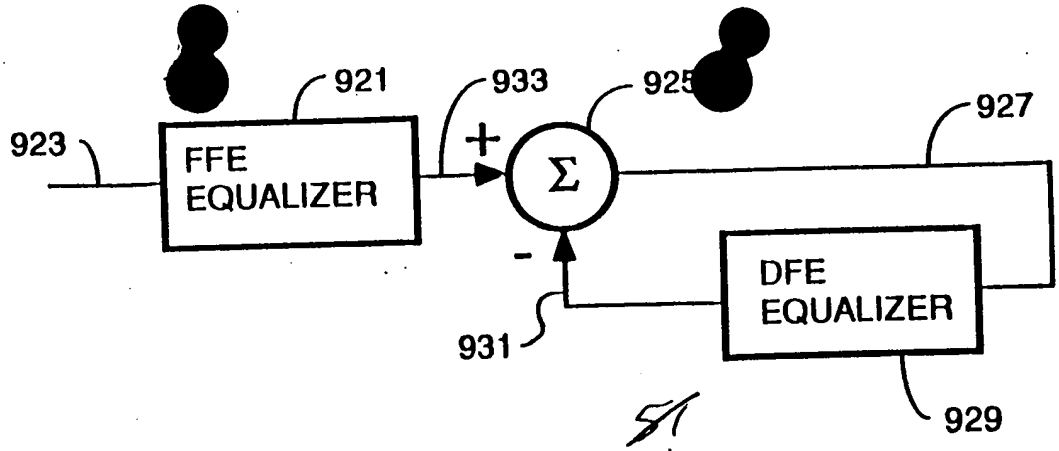


FIG. 37

50

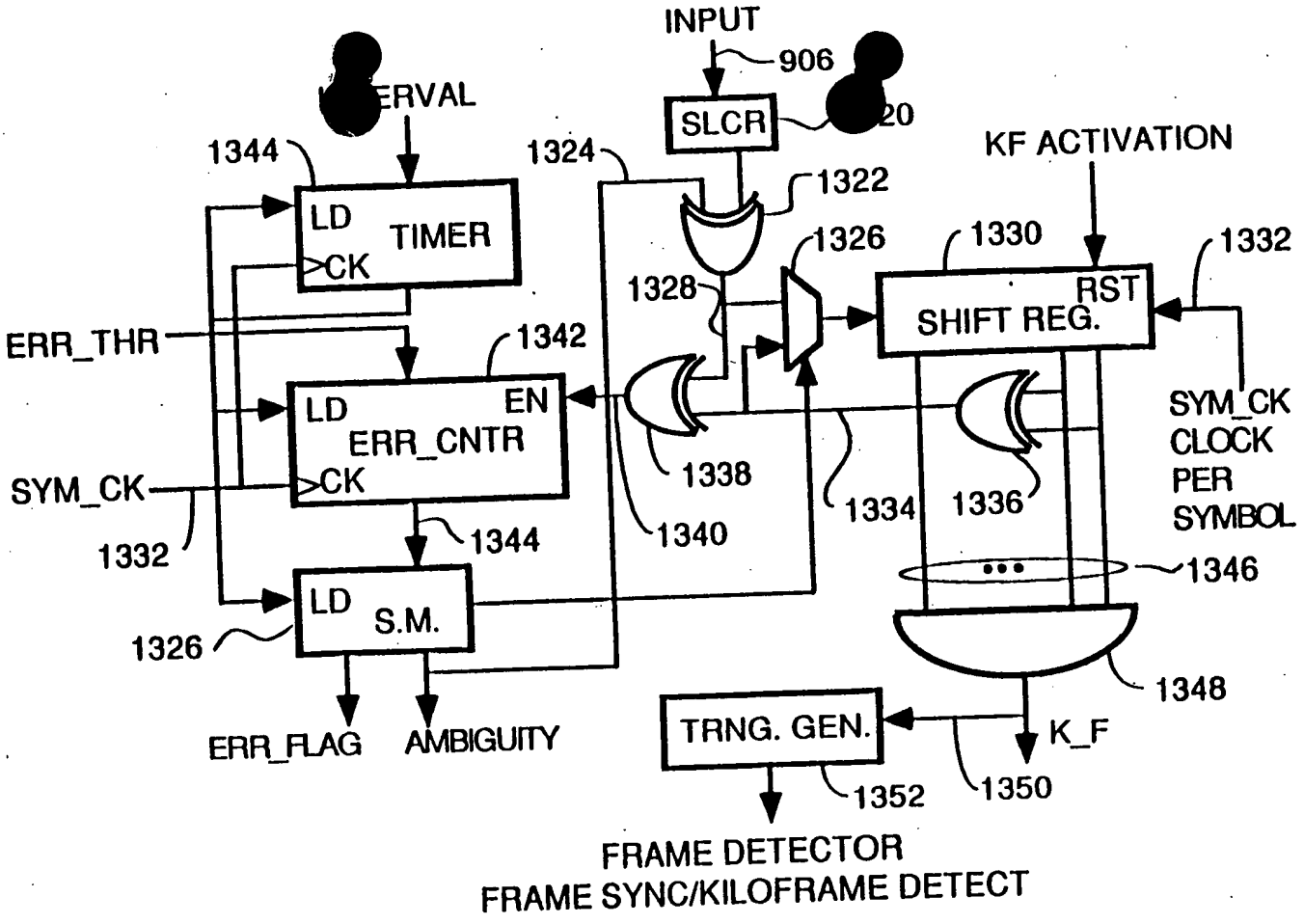
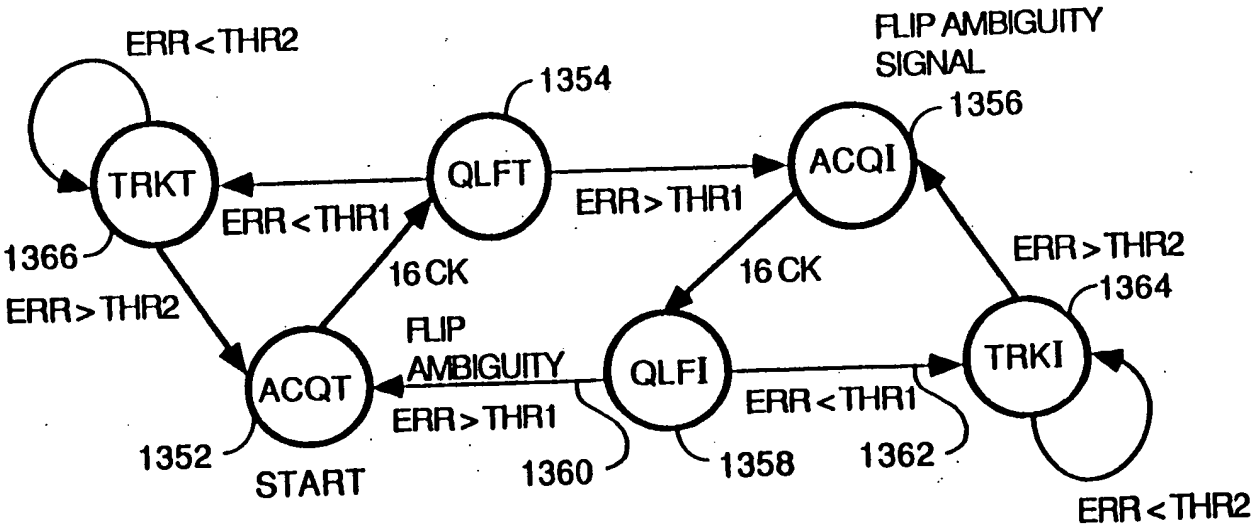


FIG. 52

51



STATE MACHINE

FIG. 53

52

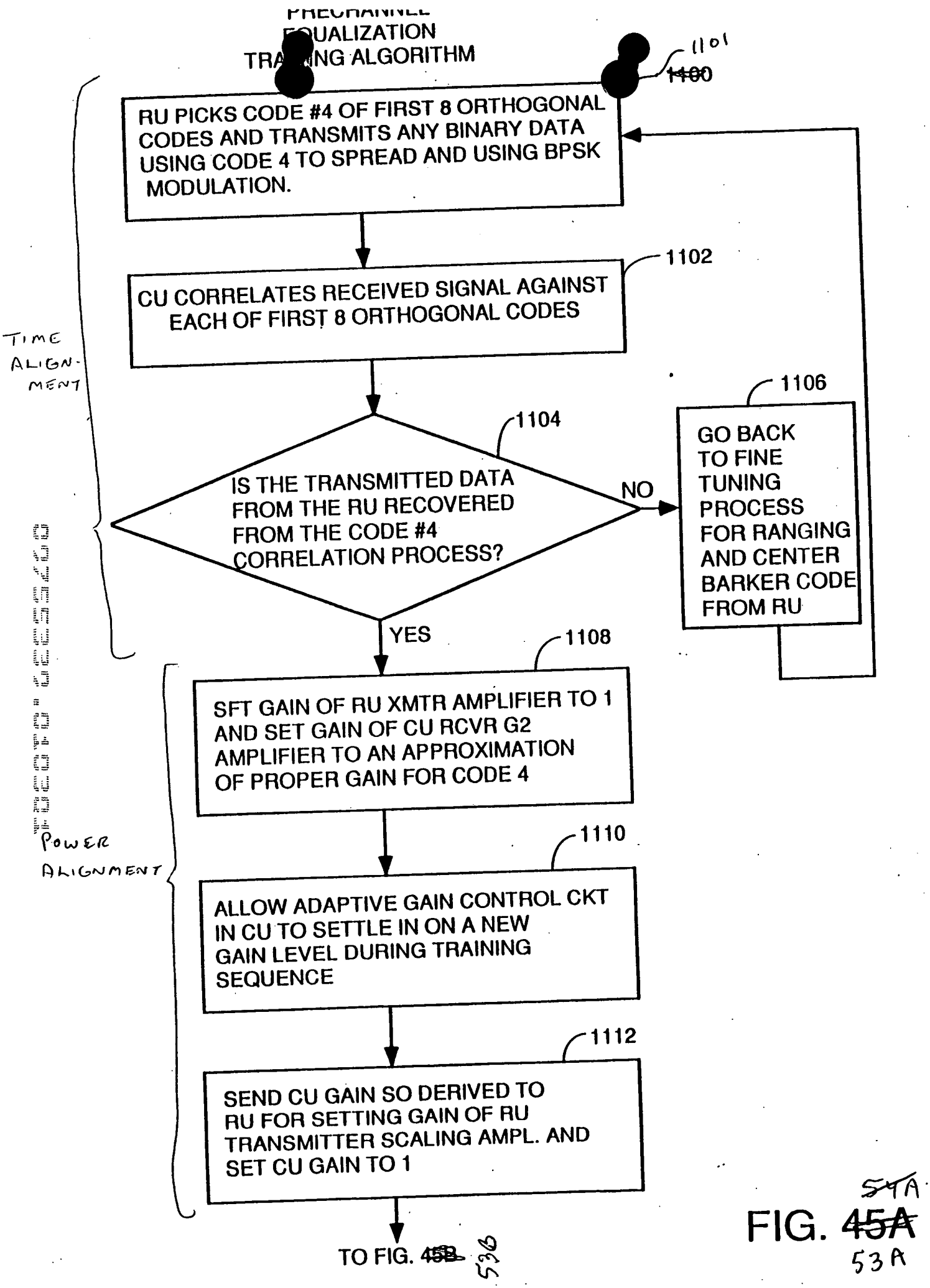

PRECHANNEL EQUALIZATION TRAINING ALGORITHM
1101
1100
RU PICKS CODE #4 OF FIRST 8 ORTHOGONAL CODES AND TRANSMITS ANY BINARY DATA USING CODE 4 TO SPREAD AND USING BPSK MODULATION.
1102
CU CORRELATES RECEIVED SIGNAL AGAINST EACH OF FIRST 8 ORTHOGONAL CODES
TIME ALIGNMENT
1104
IS THE TRANSMITTED DATA FROM THE RU RECOVERED FROM THE CODE #4 CORRELATION PROCESS?
NO
1106
GO BACK TO FINE TUNING PROCESS FOR RANGING AND CENTER BARKER CODE FROM RU
YES
1108
SFT GAIN OF RU XMTR AMPLIFIER TO 1 AND SET GAIN OF CU RCVR G2 AMPLIFIER TO AN APPROXIMATION OF PROPER GAIN FOR CODE 4
POWER ALIGNMENT
1110
ALLOW ADAPTIVE GAIN CONTROL CKT IN CU TO SETTLE IN ON A NEW GAIN LEVEL DURING TRAINING SEQUENCE
1112
SEND CU GAIN SO DERIVED TO RU FOR SETTING GAIN OF RU TRANSMITTER SCALING AMPL. AND SET CU GAIN TO 1
TO FIG. 45B
53B

FIG. 45A
53A

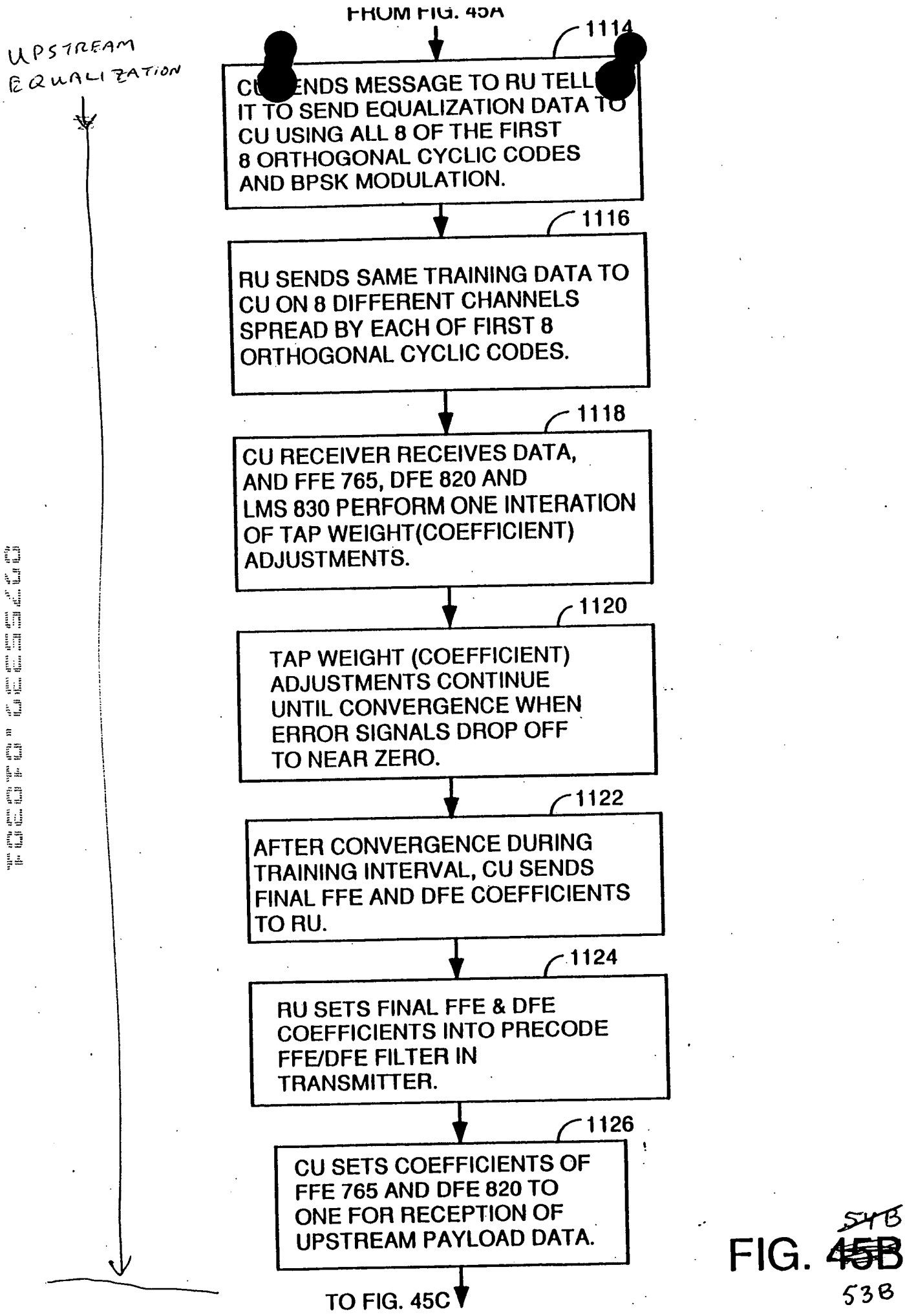

FROM FIG. 45A
UPSTREAM EQUALIZATION
1114
CU SENDS MESSAGE TO RU TELLING IT TO SEND EQUALIZATION DATA TO CU USING ALL 8 OF THE FIRST 8 ORTHOGONAL CYCLIC CODES AND BPSK MODULATION.
1116
RU SENDS SAME TRAINING DATA TO CU ON 8 DIFFERENT CHANNELS SPREAD BY EACH OF FIRST 8 ORTHOGONAL CYCLIC CODES.
1118
CU RECEIVER RECEIVES DATA, AND FFE 765, DFE 820 AND LMS 830 PERFORM ONE INTERATION OF TAP WEIGHT(COEFFICIENT) ADJUSTMENTS.
1120
TAP WEIGHT (COEFFICIENT) ADJUSTMENTS CONTINUE UNTIL CONVERGENCE WHEN ERROR SIGNALS DROP OFF TO NEAR ZERO.
1122
AFTER CONVERGENCE DURING TRAINING INTERVAL, CU SENDS FINAL FFE AND DFE COEFFICIENTS TO RU.
1124
RU SETS FINAL FFE & DFE COEFFICIENTS INTO PRECODE FFE/DFE FILTER IN TRANSMITTER.
1126
CU SETS COEFFICIENTS OF FFE 765 AND DFE 820 TO ONE FOR RECEPTION OF UPSTREAM PAYLOAD DATA.
TO FIG. 45C

FIG. 45B

53B

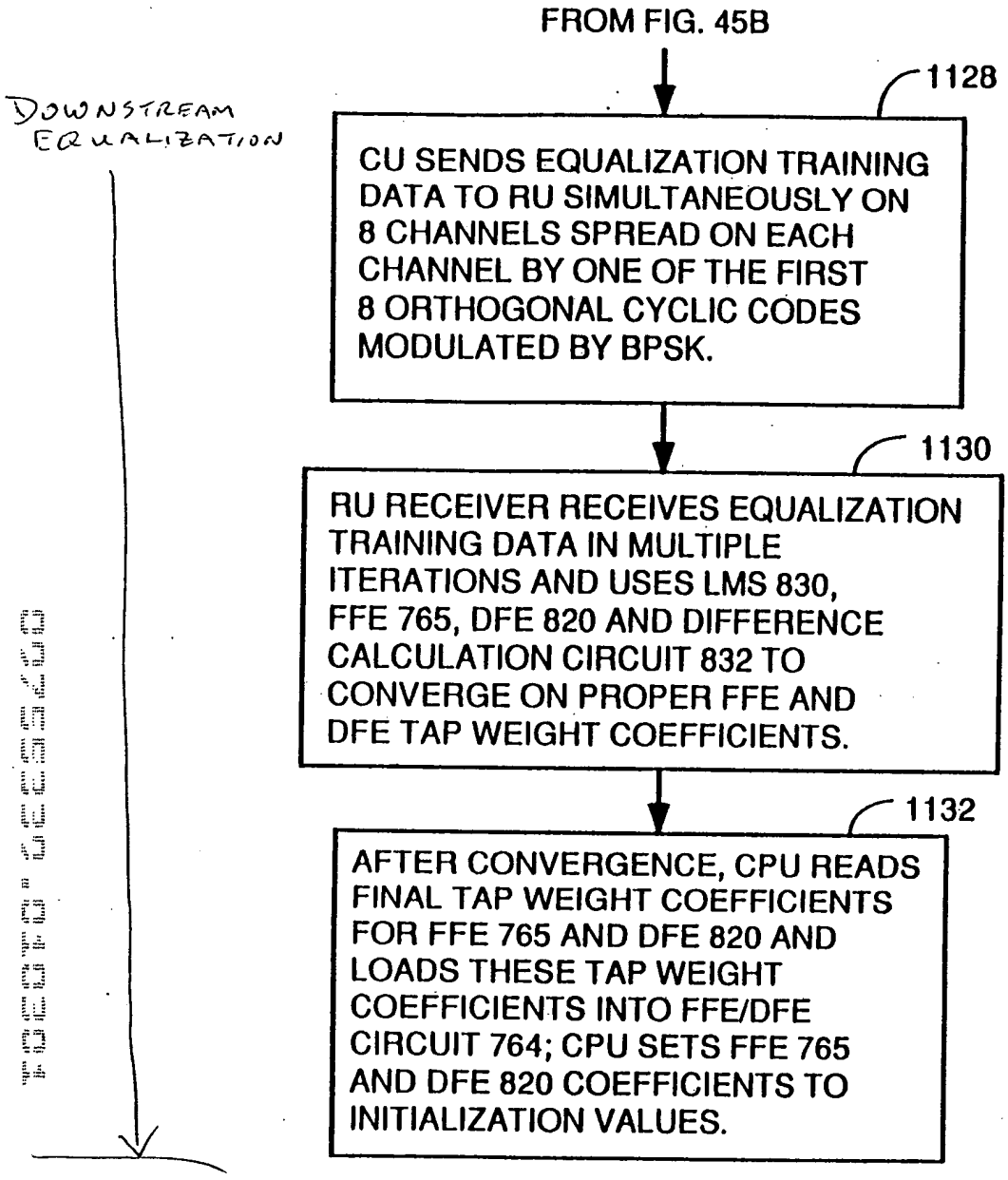

FROM FIG. 45B
DOWNSTREAM EQUALIZATION
1128
CU SENDS EQUALIZATION TRAINING DATA TO RU SIMULTANEOUSLY ON 8 CHANNELS SPREAD ON EACH CHANNEL BY ONE OF THE FIRST 8 ORTHOGONAL CYCLIC CODES MODULATED BY BPSK.
1130
RU RECEIVER RECEIVES EQUALIZATION TRAINING DATA IN MULTIPLE ITERATIONS AND USES LMS 830, FFE 765, DFE 820 AND DIFFERENCE CALCULATION CIRCUIT 832 TO CONVERGE ON PROPER FFE AND DFE TAP WEIGHT COEFFICIENTS.
1132
AFTER CONVERGENCE, CPU READS FINAL TAP WEIGHT COEFFICIENTS FOR FFE 765 AND DFE 820 AND LOADS THESE TAP WEIGHT COEFFICIENTS INTO FFE/DFE CIRCUIT 764; CPU SETS FFE 765 AND DFE 820 COEFFICIENTS TO INITIALIZATION VALUES.

FIG. 45C

53C

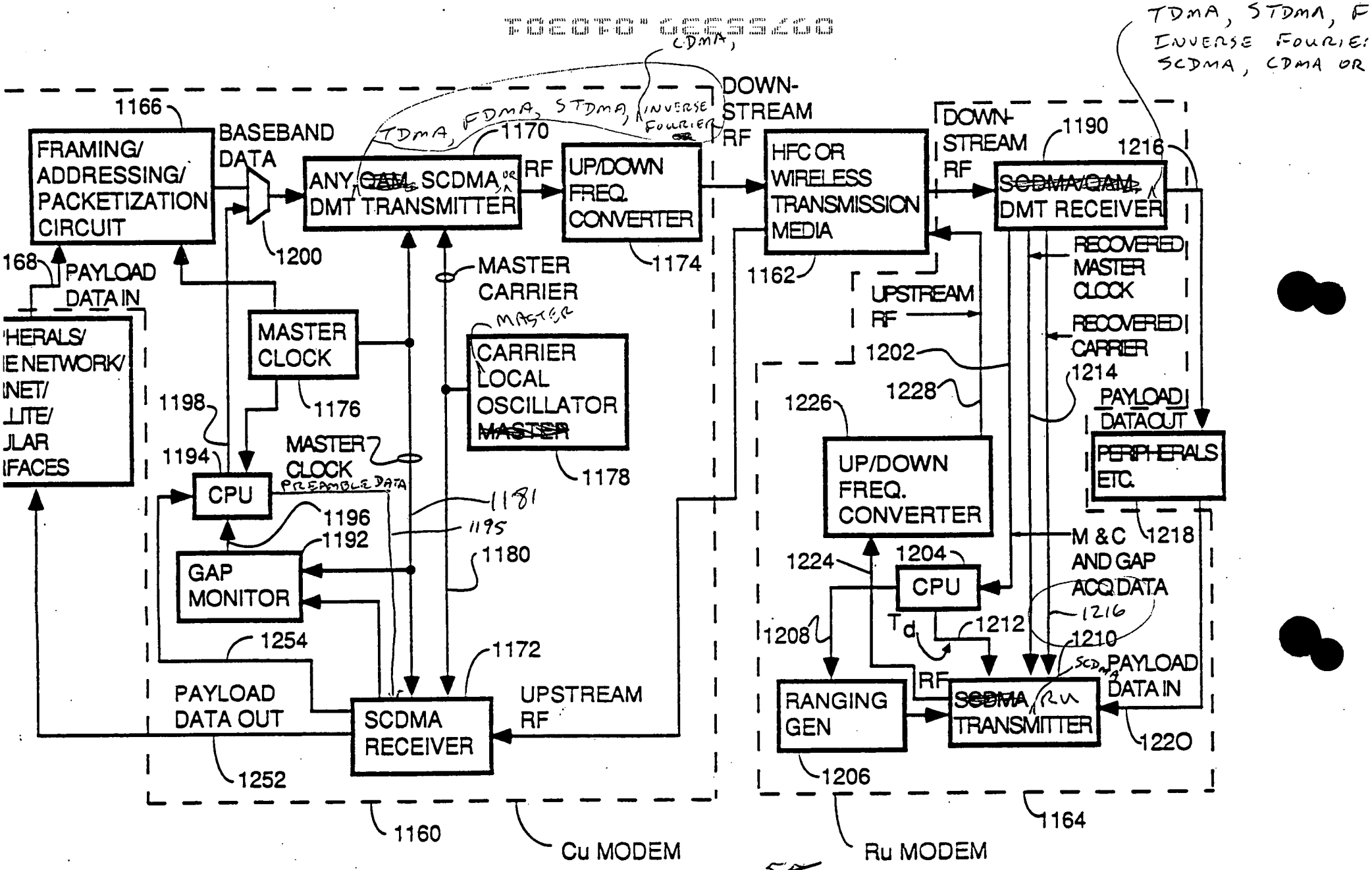
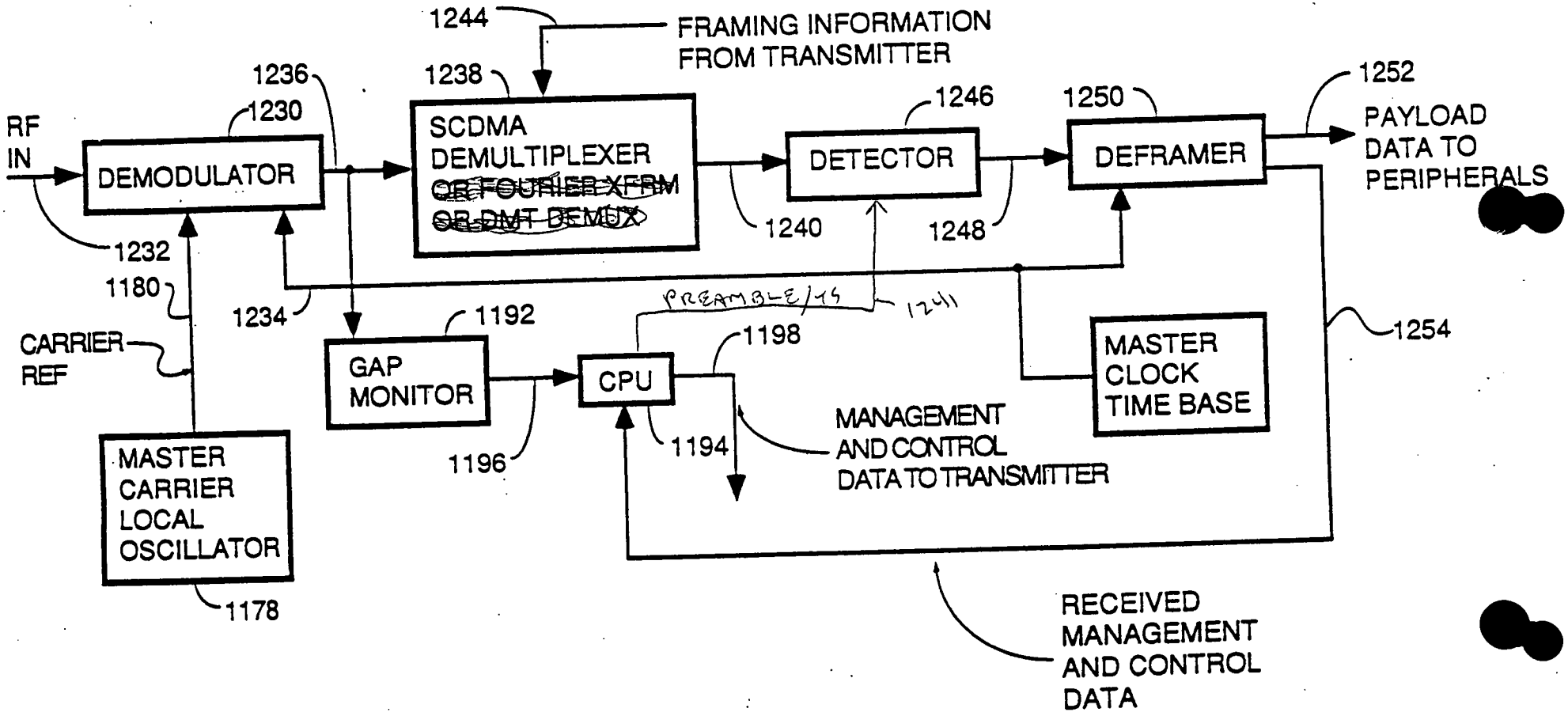

1166
FRAMING/ ADDRESSING/ PACKETIZATION CIRCUIT
BASEBAND DATA
1170
ANY SCDMA DMT TRANSMITTER
RF
UP/DOWN FREQ. CONVERTER
1174
DOWN-STREAM RF
HFC OR WIRELESS TRANSMISSION MEDIA
1162
DOWN-STREAM RF
1190
1216
SCDMA DMT RECEIVER
1200
168
PAYLOAD DATA IN
MASTER CARRIER
RECOVERED MASTER CLOCK
UPSTREAM RF
1202
RECOVERED CARRIER
1214
1228
PAYLOAD DATA OUT
PERIPHERALS ETC.
1218
MASTER CLOCK
1176
CARRIER LOCAL OSCILLATOR
1178
1198
1194
MASTER CLOCK
PREAMBLE DATA
1181
1195
1196
1192
CPU
1226
UP/DOWN FREQ. CONVERTER
1224
1204
CPU
M & C AND GAP ACQ DATA
1216
1210
1180
GAP MONITOR
1208
Td
1212
1254
1172
PAYLOAD DATA IN
RF
RANGING GEN
SCDMA TRANSMITTER
1220
PAYLOAD DATA OUT
UPSTREAM RF
SCDMA RECEIVER
1252
1206
1160
Cu MODEM
1164
Ru MODEM

FIG. 49

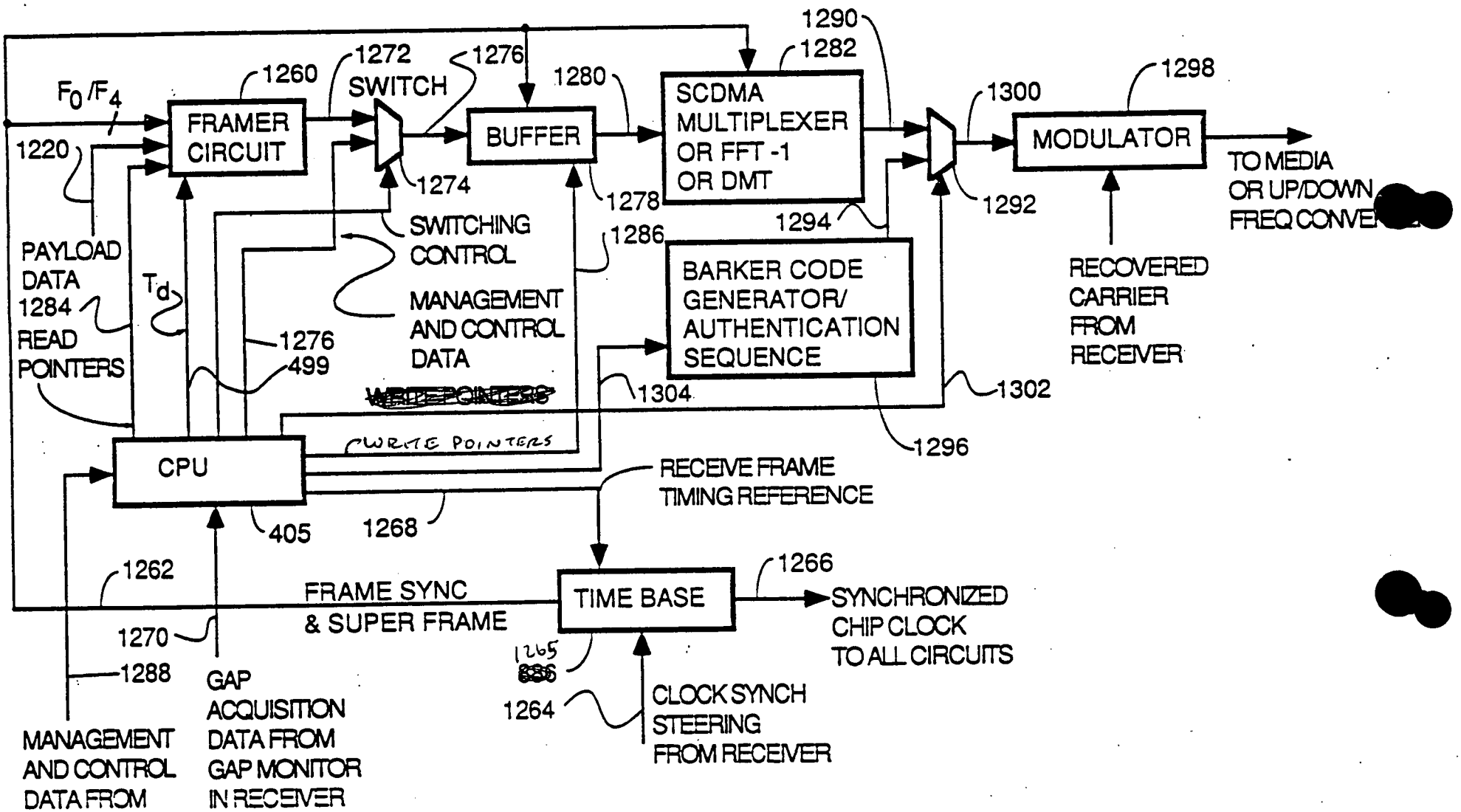
54



SIMPLE Cu SPREAD SPECTRUM RECEIVER

FIG. 50 56

55

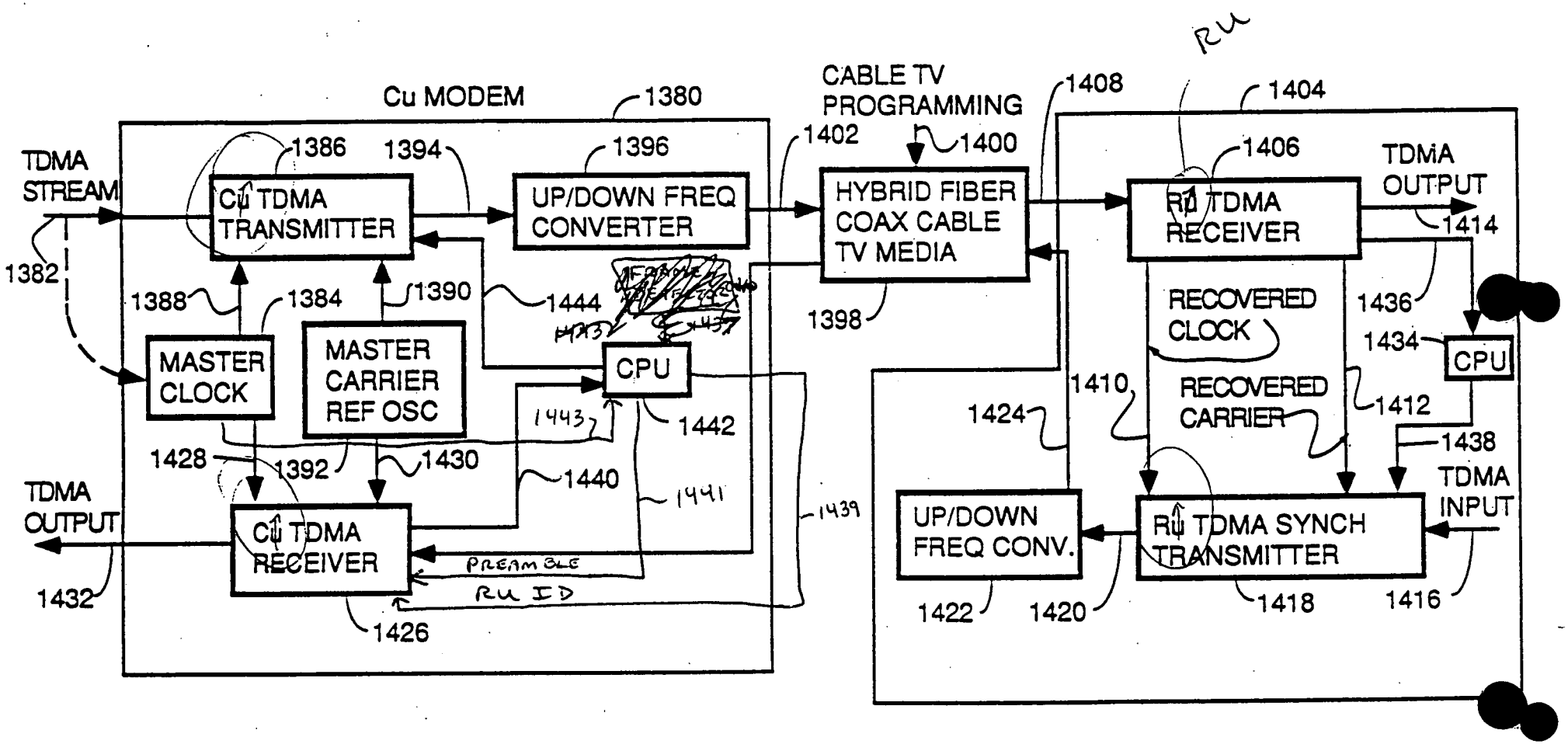


SIMPLE Ru SPREAD SPECTRUM TRANSMITTER

FIG. 51

57

56



SYNCHRONOUS TDMA SYSTEM

FIG. 54

57

OFFSET	1B ASIC		2A ASIC	
(Chips)	RGSRH	RGSRL	RGSRH	RGSRL
0	0x0000	0x8000	0x0001	0x0000
1/2	0x0000	0xC000	0x0001	0x8000
1	0x0000	0x4000	0x0000	0x8000
-1	0x0001	0x0000	0x0002	0x0000

FIG. 58

Training Algorithm

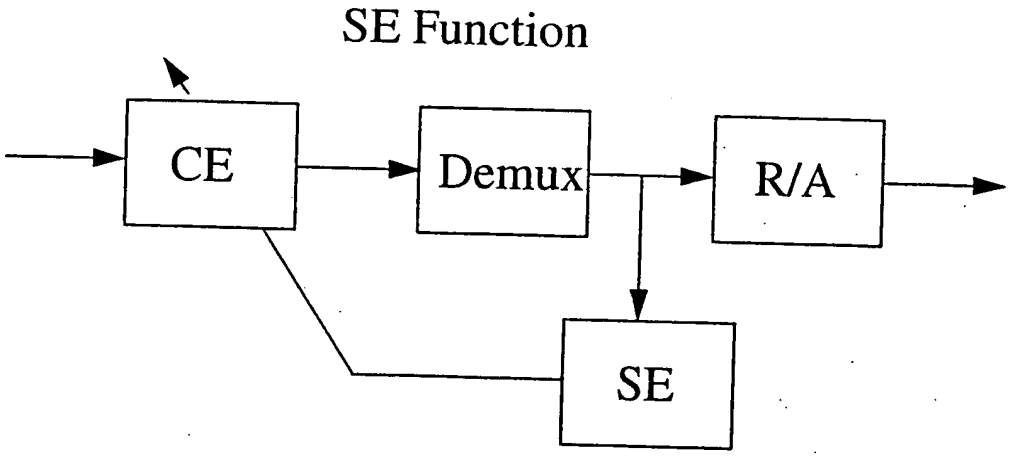
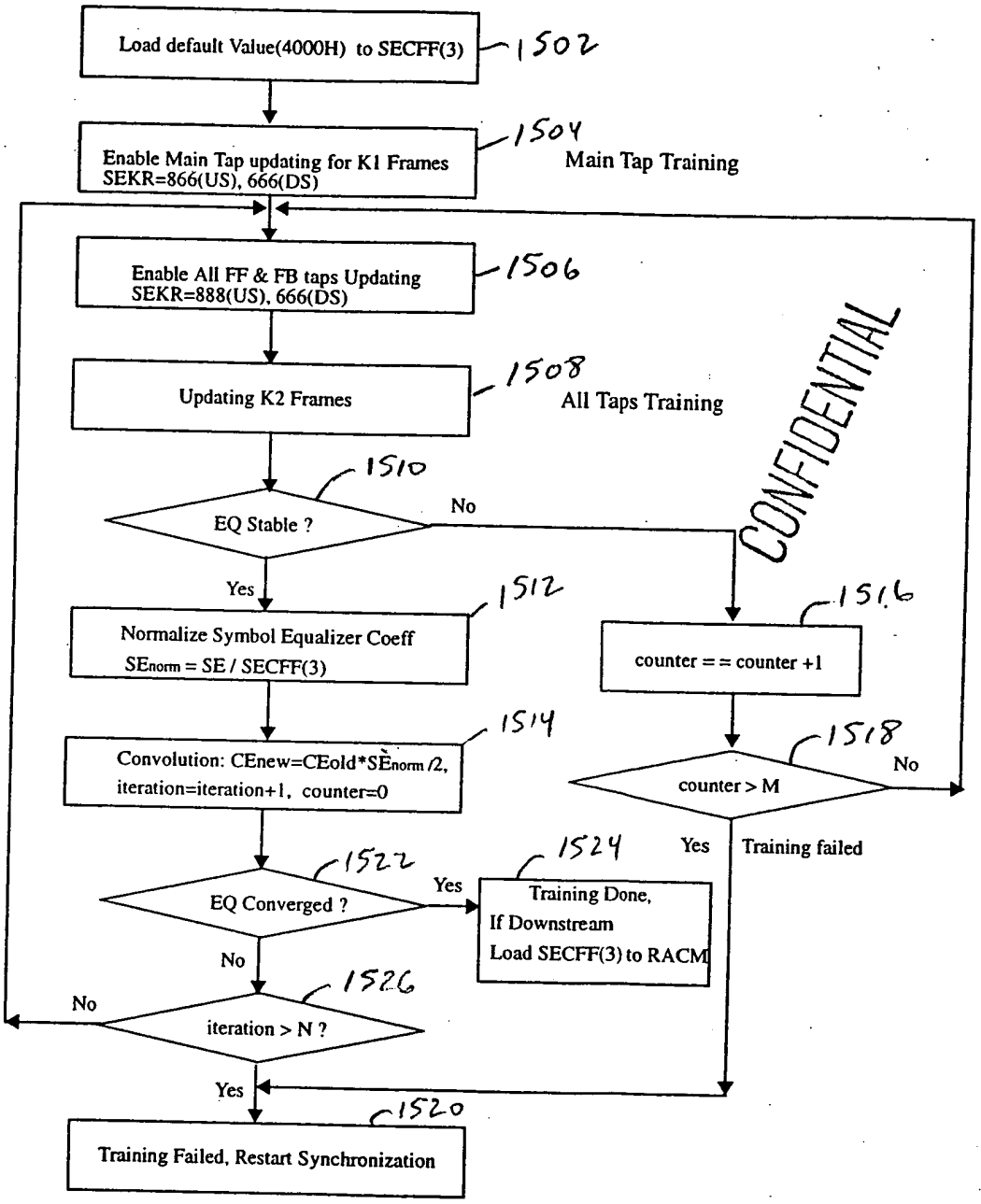


FIG. 59

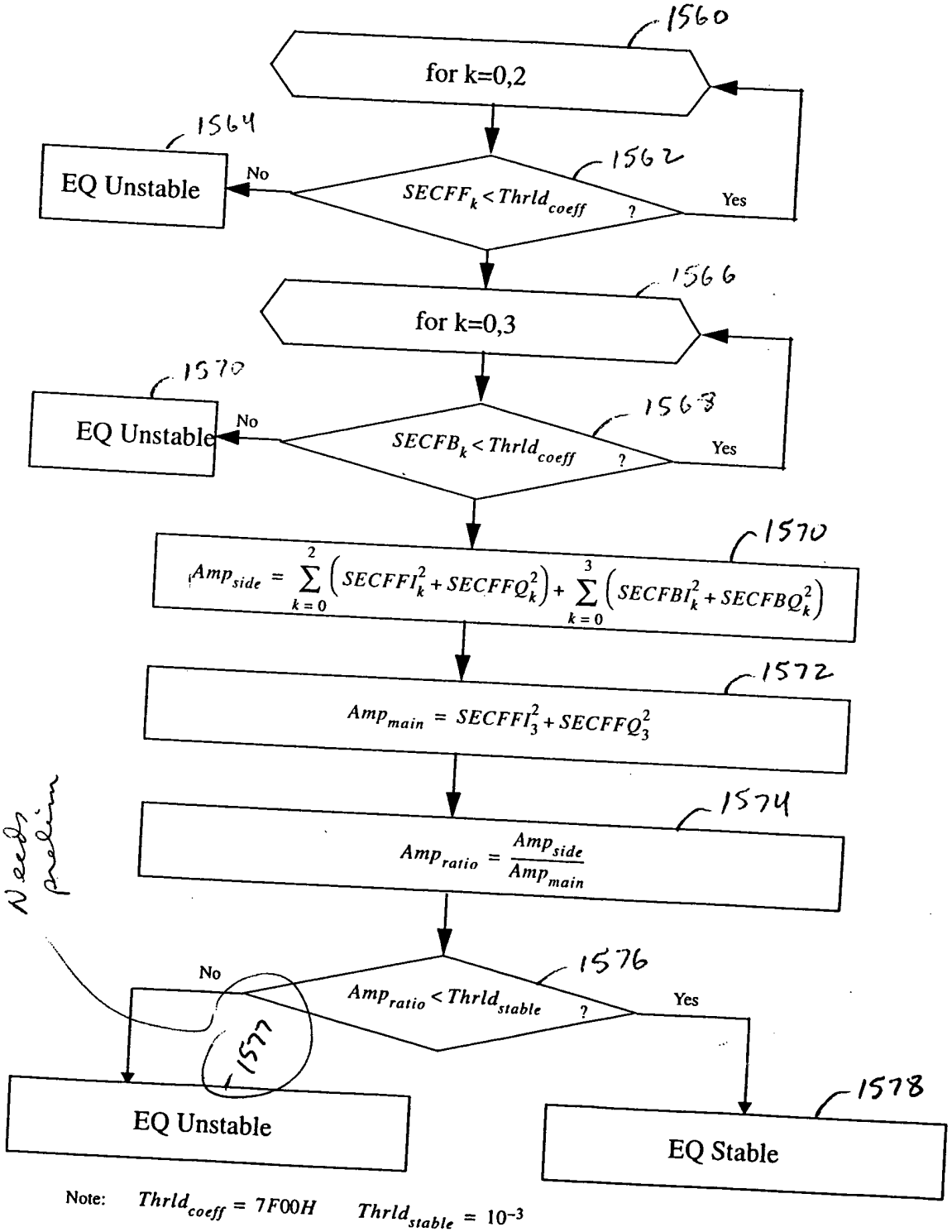
Initial 2-Step Training Algorithm



2-STEP INITIAL EQUALIZATION TRAINING

FIG. 60

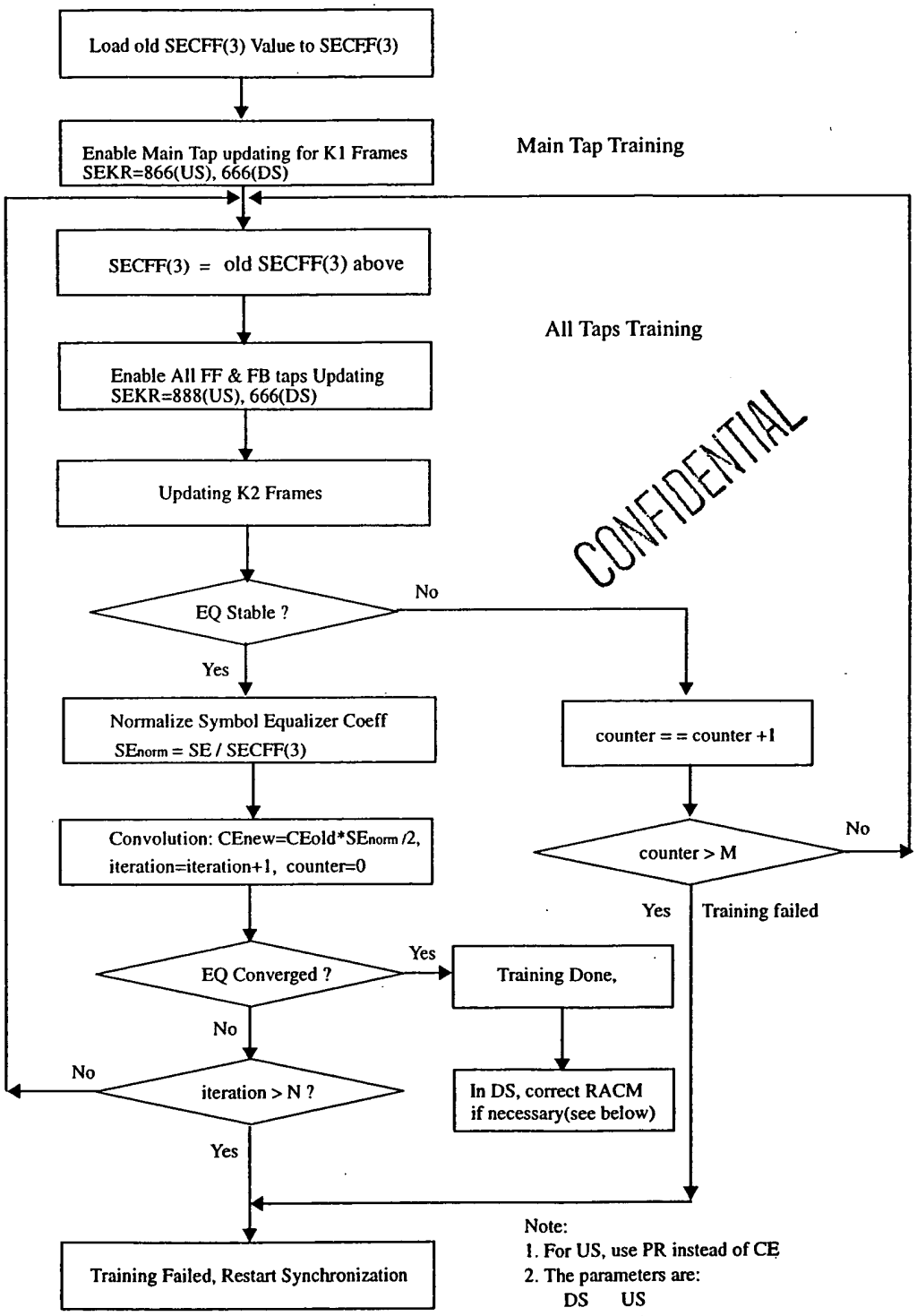
EQ Stability Check



Note: $Thrld_{coeff} = 7F00H$ $Thrld_{stable} = 10^{-3}$

FIG. 61

Periodic 2-Step Training Algorithm

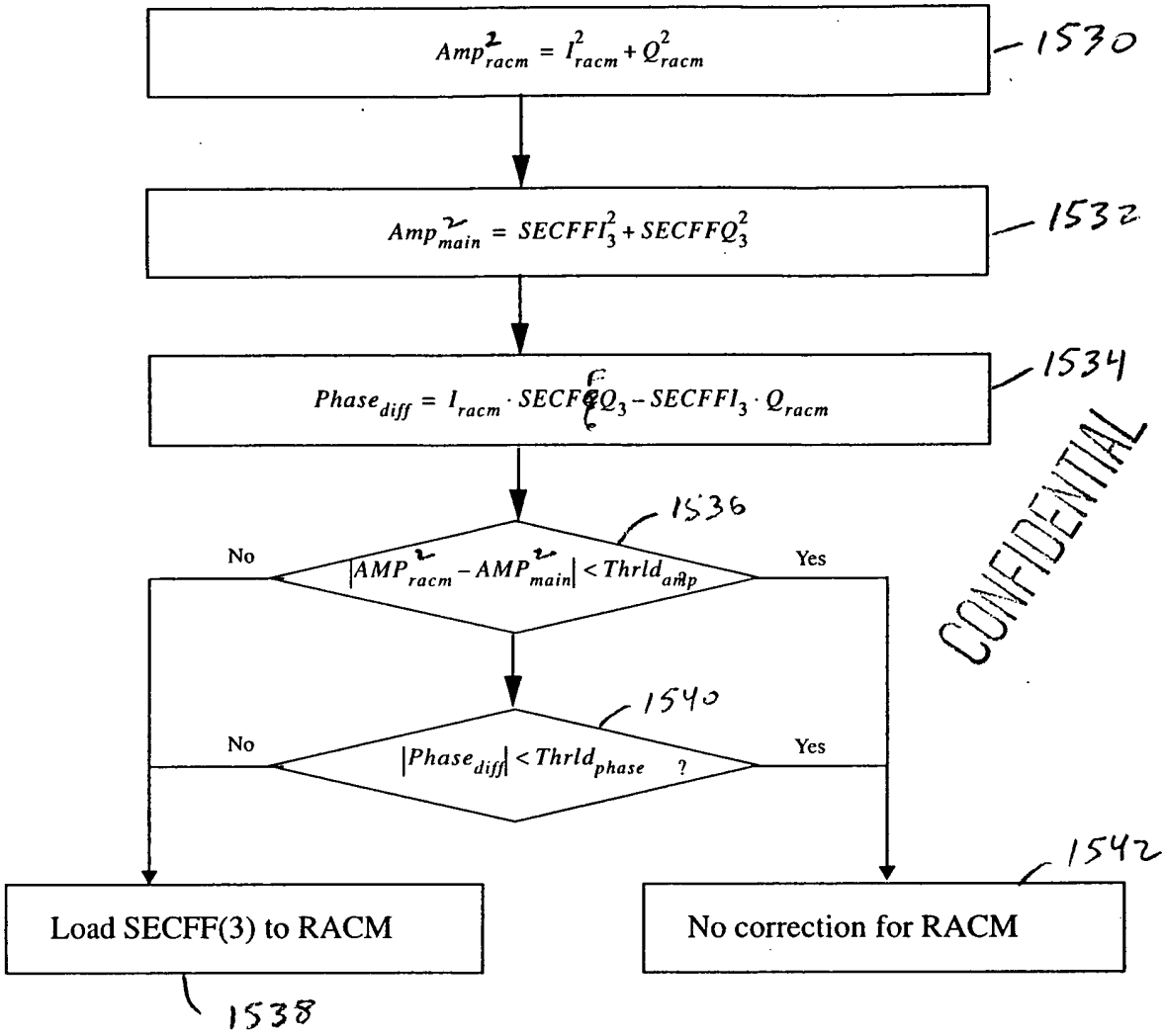


Note:
1. For US, use PR instead of CE
2. The parameters are:

	DS	US
K1	30	30
K2	20	30
N	5	3
M	3	3

FIG. 62

RACM Correction



CONFIDENTIAL

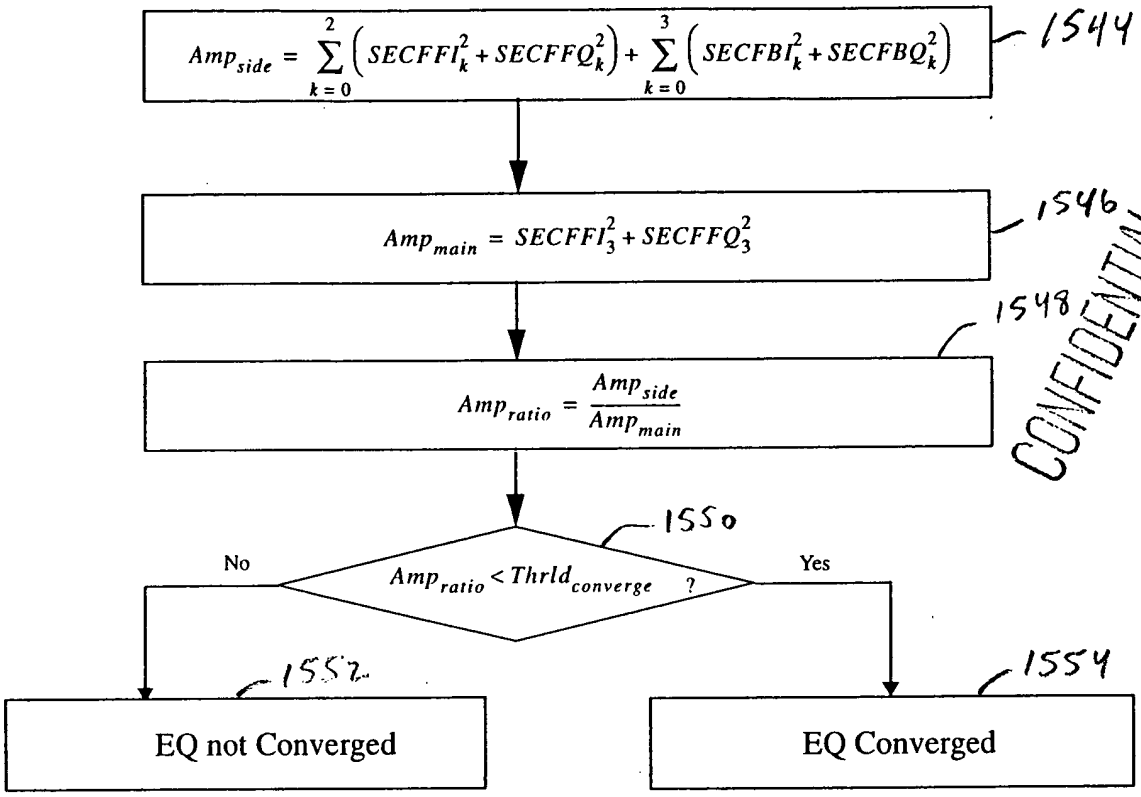
Note: $Thrld_{amp} = TBD$

$Thrld_{phase} = TBD$

ROTATIONAL AMPLIFIER CORRECTION

FIG. 63

EQ Convergence Check



Note: $Thrld_{converge} = 10^{-5}$

FIG. 64

Power Alignment Flow Chart

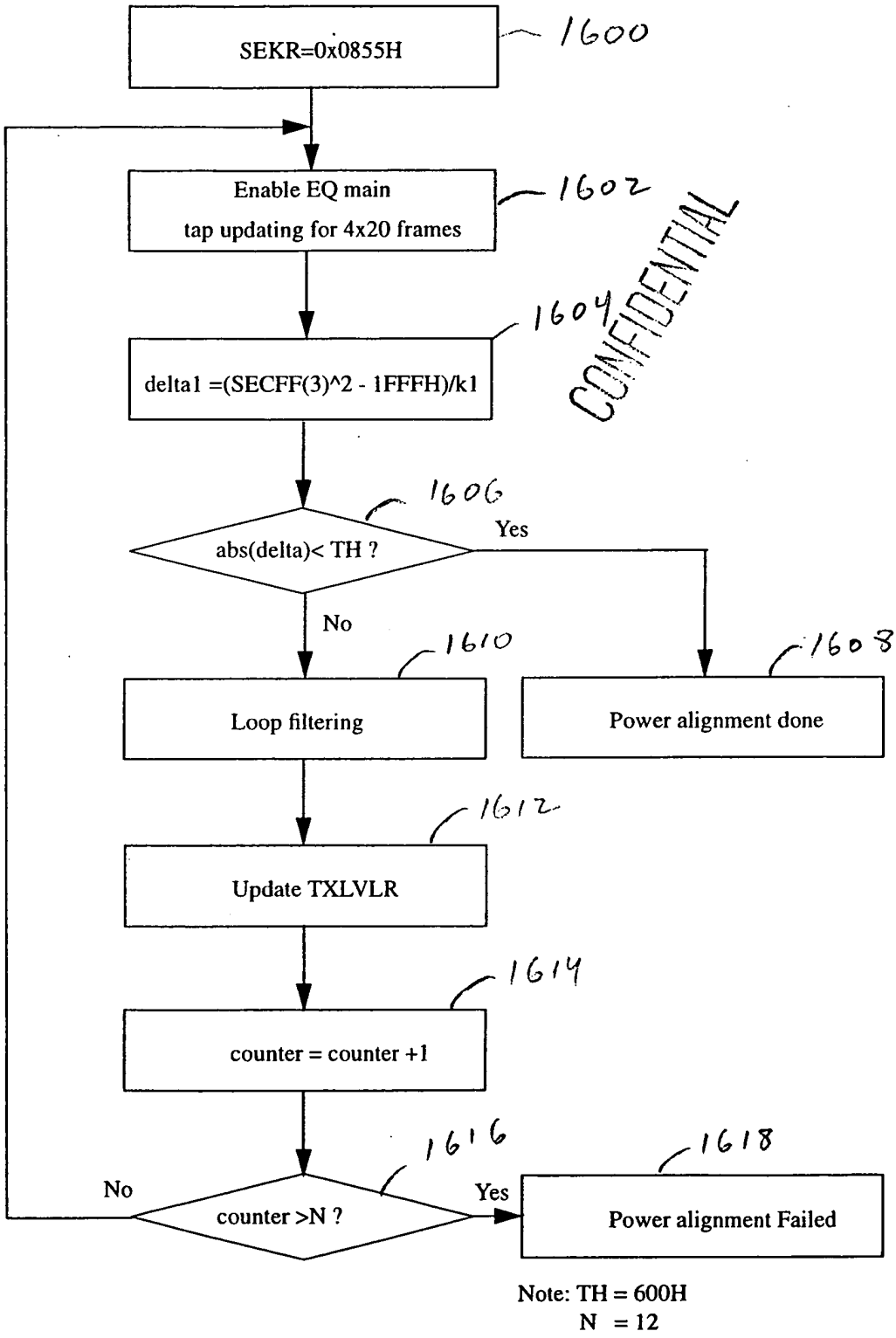


FIG. 65

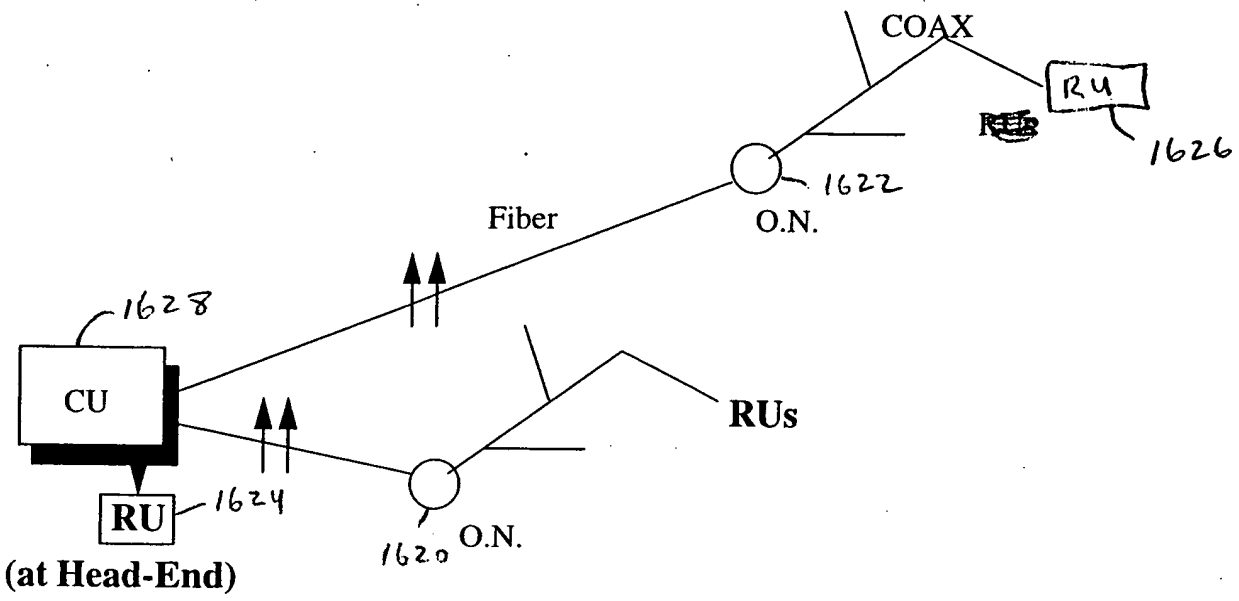
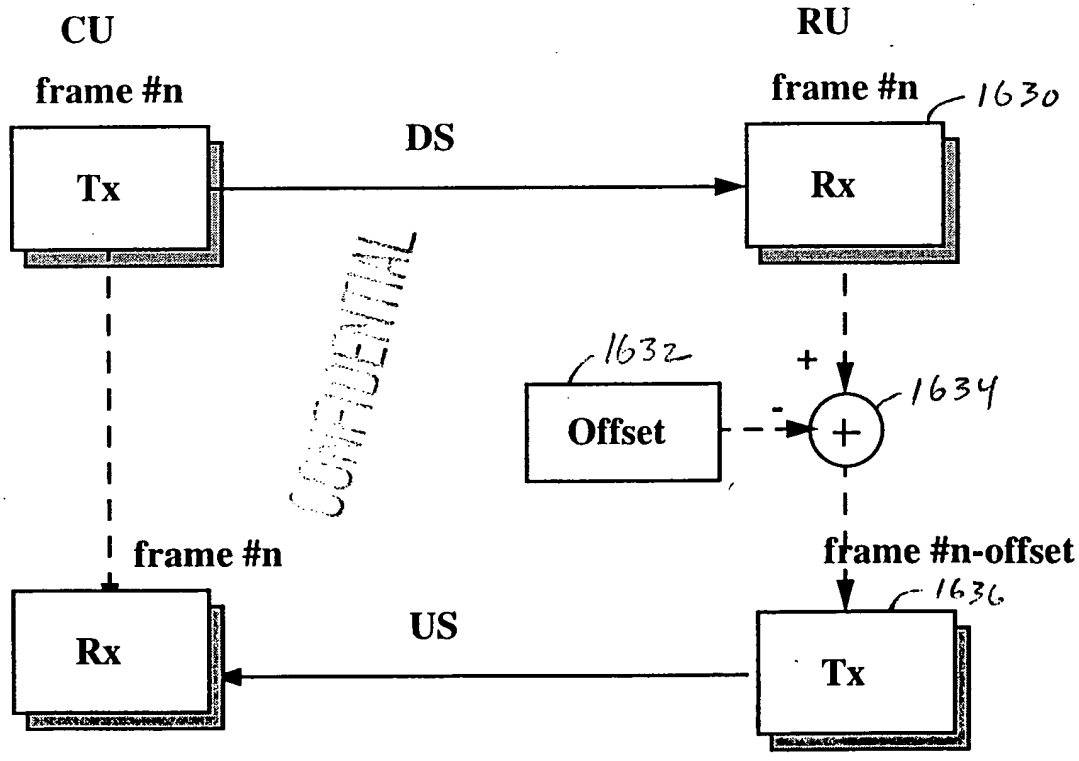


FIG. 66



Total Turn Around (TTA) in frames = Offset

FIG. 67

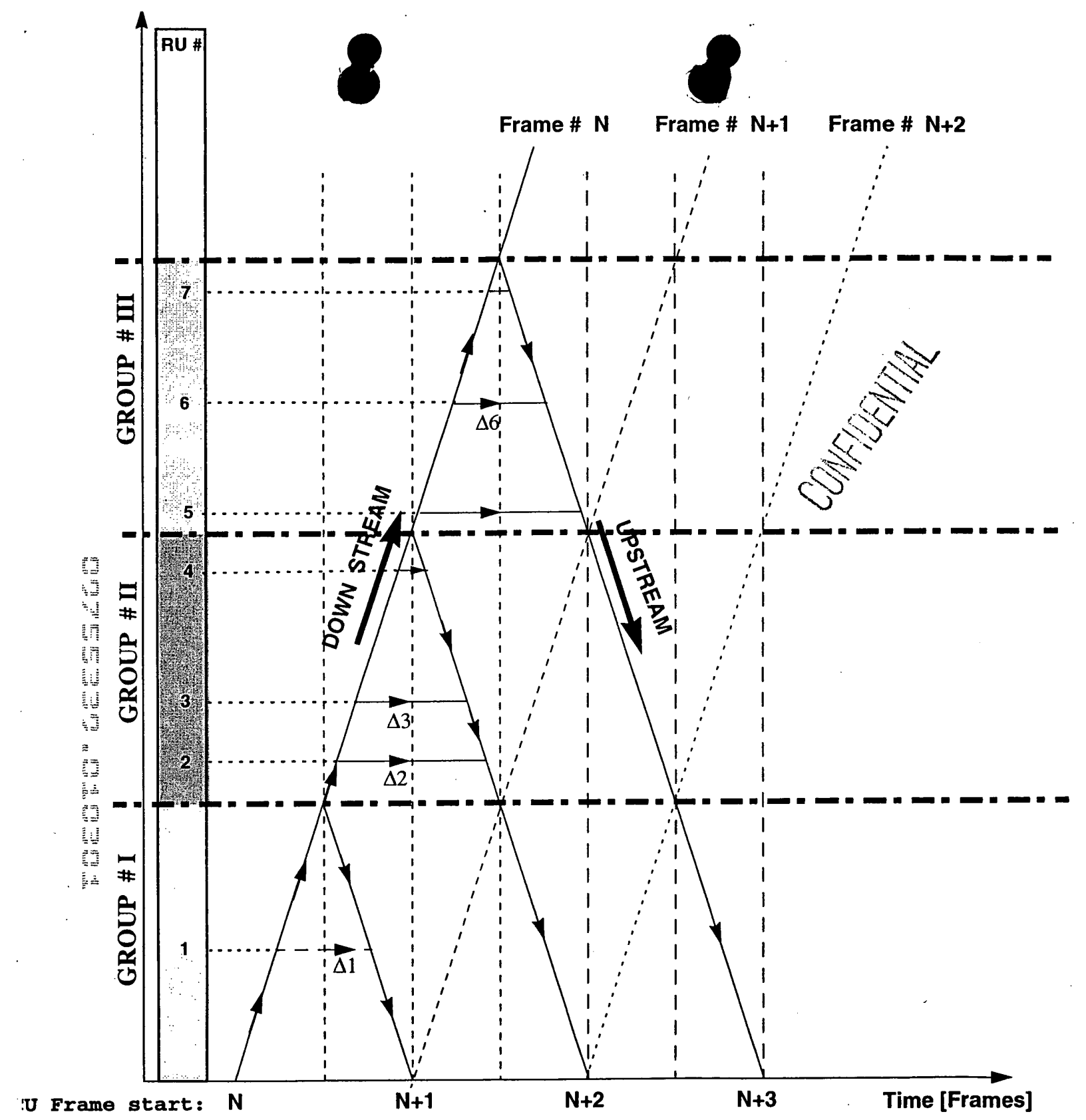


FIG. 6B

Figure 3-1: Frame start propagation along the channel

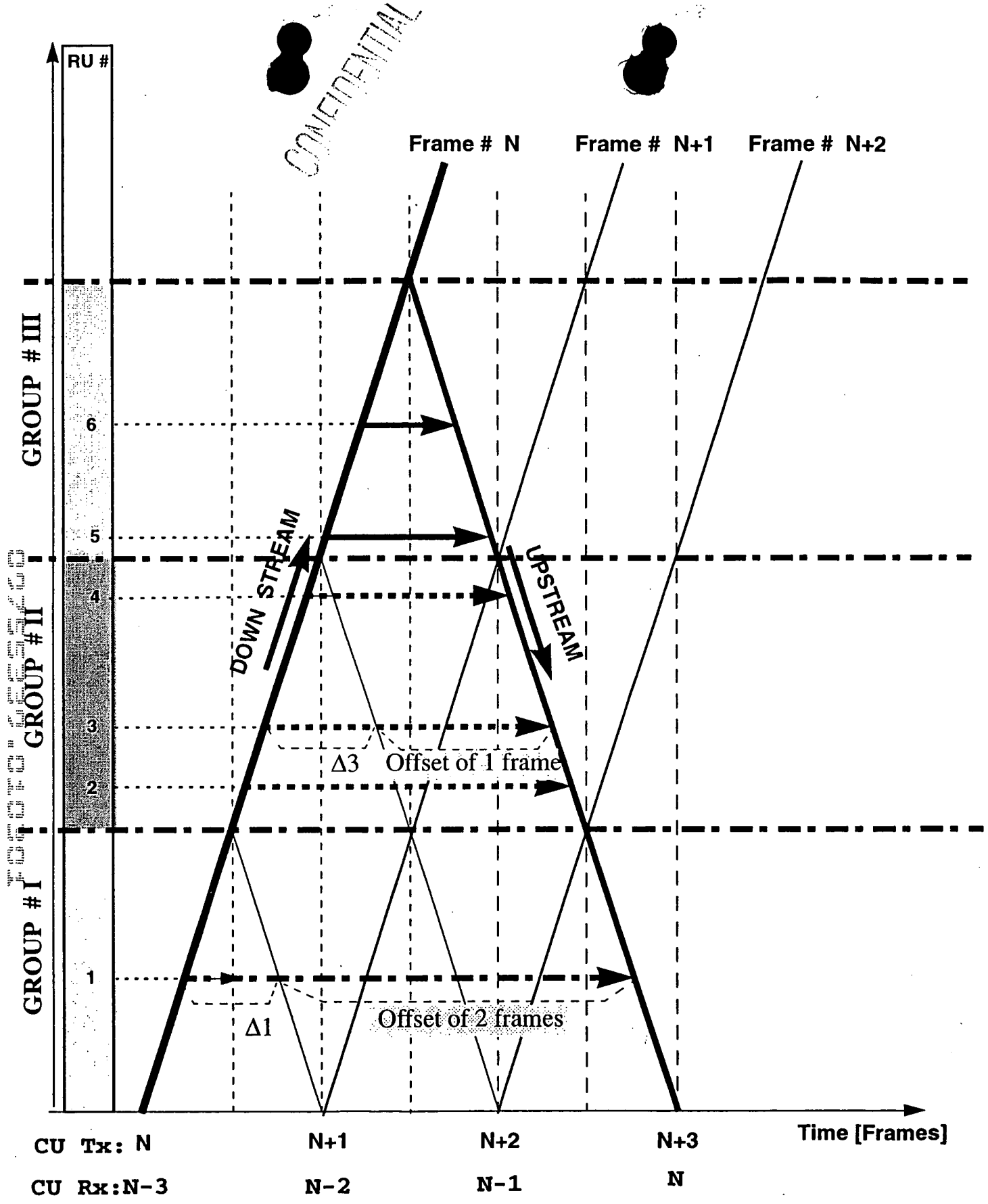


FIG. 69

Figure 69 Control message (downstream) and function (upstream) propagation in a 3 frames TTA channel

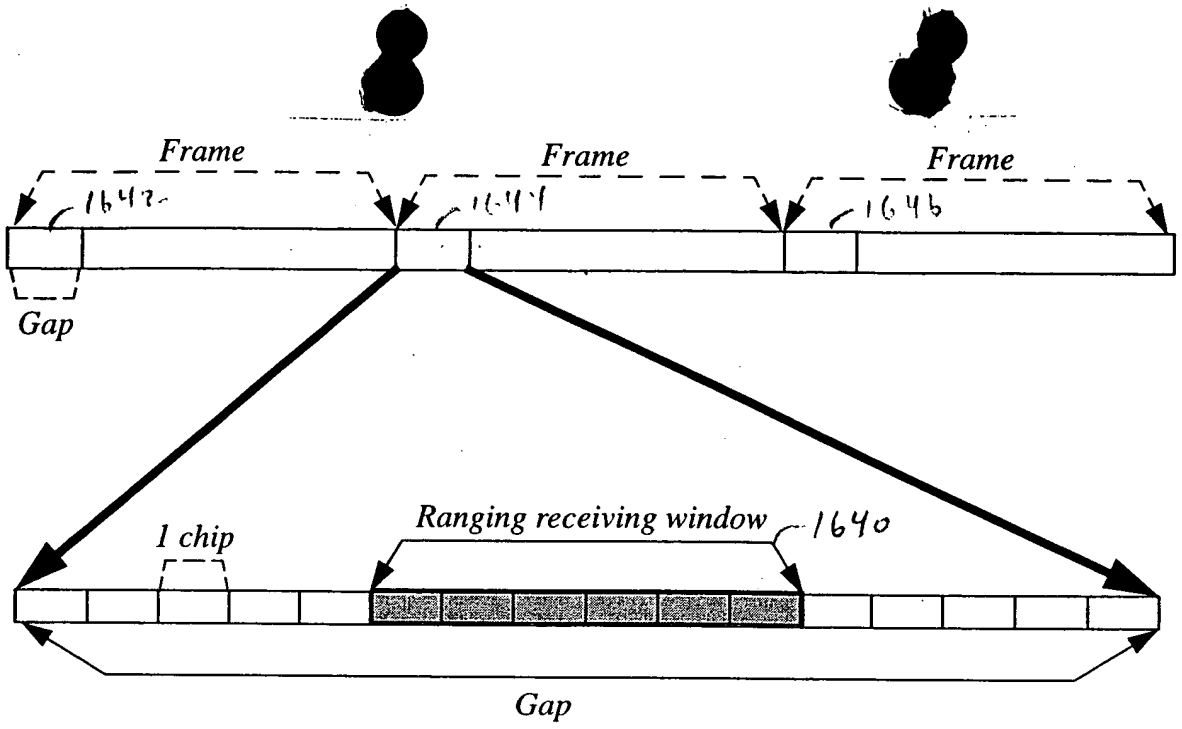

Frame
Frame
Frame
1642
1644
1646
Gap
1 chip
Ranging receiving window
1640
Gap

FIG. 7D

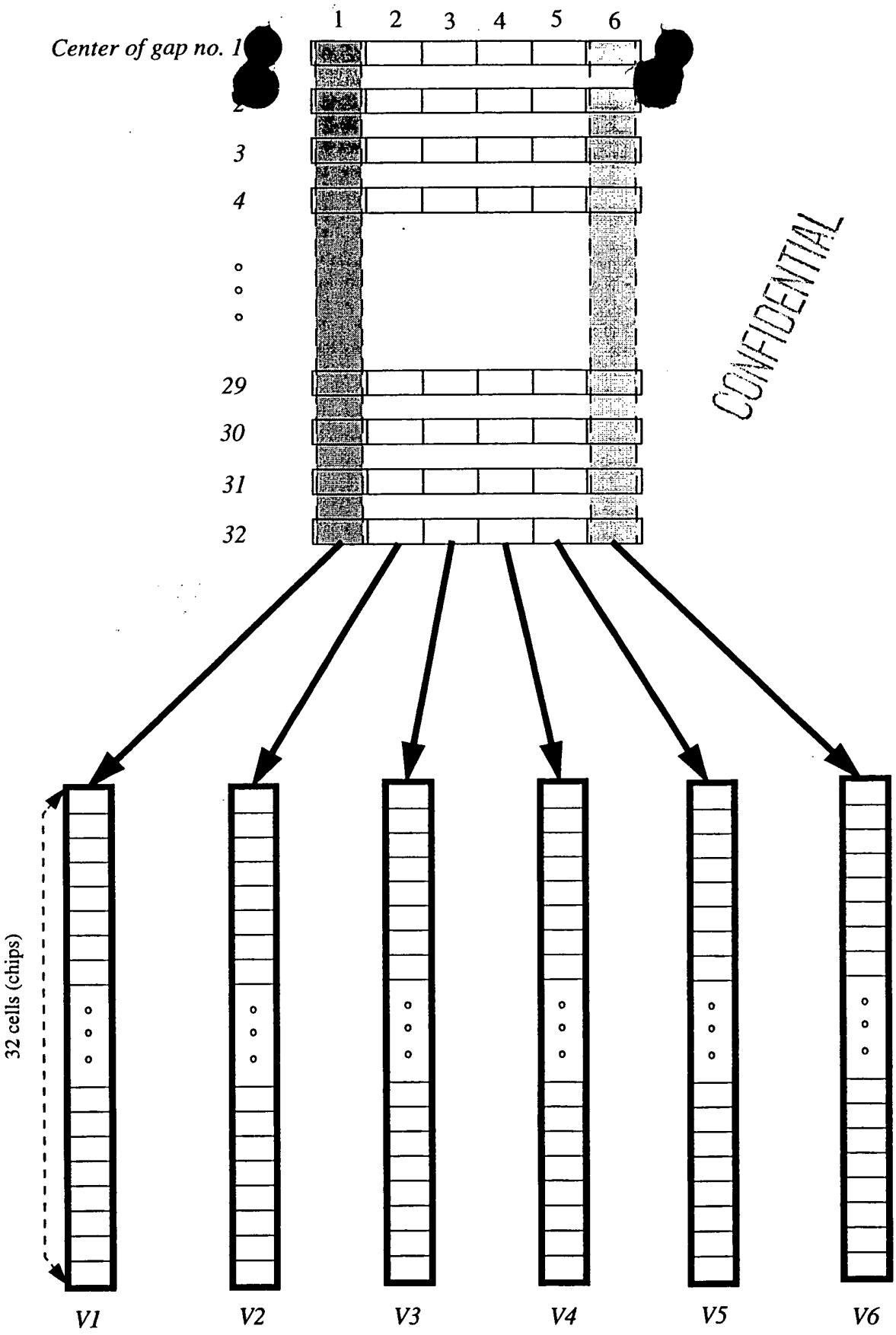


Figure 3.4: Overall view of the CU sensing windows in a "boundless ranging" algorithm

FIG. 71

Chip\FR	1	2	3	4	5	6	7		33
1	0	0	1	0	0	1	1	...	0
2	1	0	0	1	1	1	1	...	
3	0	0	0	1	1	1			
4	0	0	0	1	0	0	0	...	0
5	0	1	0	0	1				
6	0	0	1	1	1				
7	0	0	0	1	1				
8	0	0	0	0	1	0	0	...	

FIG. 72

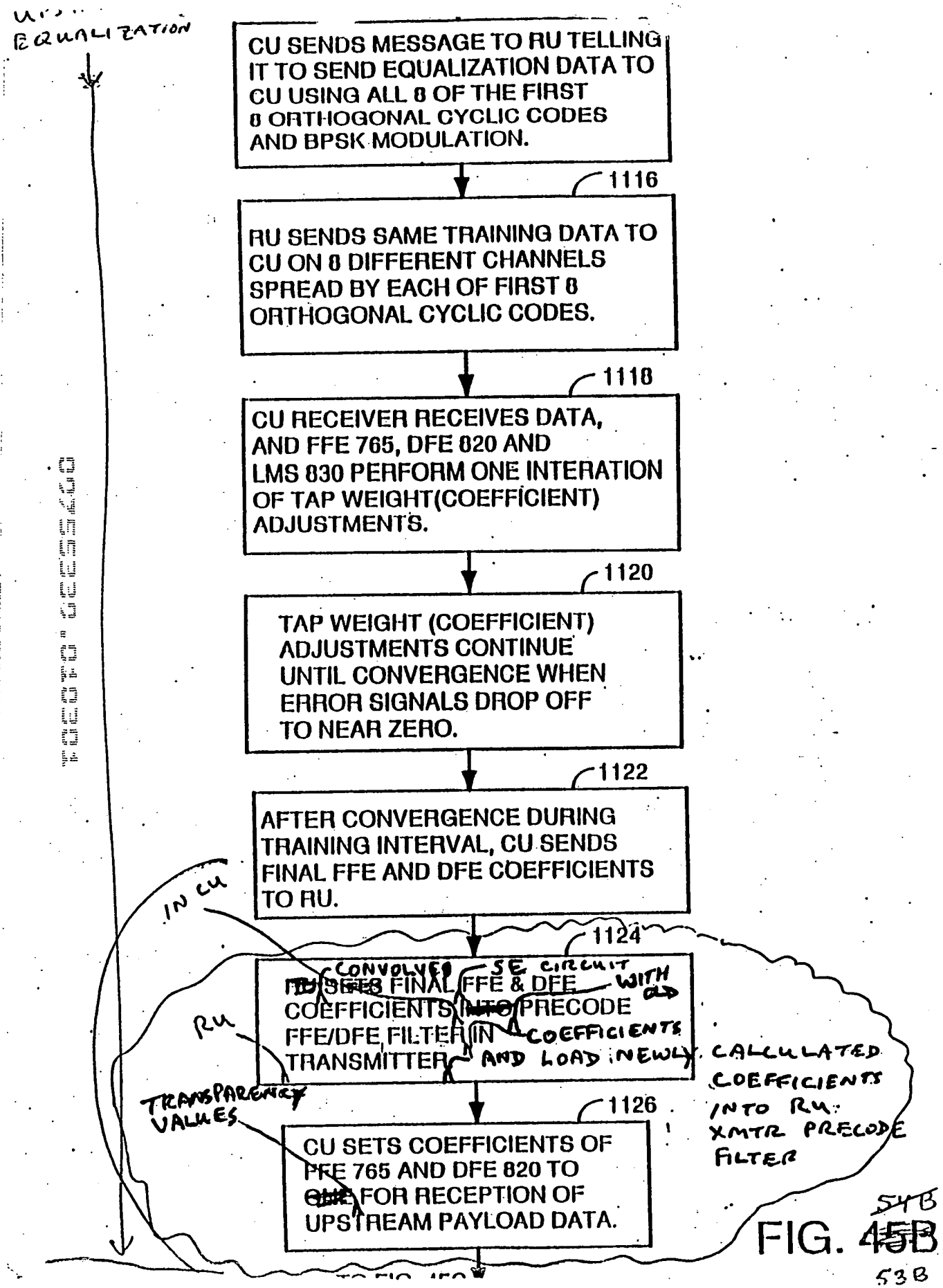

EQUALIZATION
CU SENDS MESSAGE TO RU TELLING IT TO SEND EQUALIZATION DATA TO CU USING ALL 8 OF THE FIRST 8 ORTHOGONAL CYCLIC CODES AND BPSK MODULATION.
1116
RU SENDS SAME TRAINING DATA TO CU ON 8 DIFFERENT CHANNELS SPREAD BY EACH OF FIRST 8 ORTHOGONAL CYCLIC CODES.
1118
CU RECEIVER RECEIVES DATA, AND FFE 765, DFE 820 AND LMS 830 PERFORM ONE INTERATION OF TAP WEIGHT(COEFFICIENT) ADJUSTMENTS.
1120
TAP WEIGHT (COEFFICIENT) ADJUSTMENTS CONTINUE UNTIL CONVERGENCE WHEN ERROR SIGNALS DROP OFF TO NEAR ZERO.
1122
AFTER CONVERGENCE DURING TRAINING INTERVAL, CU SENDS FINAL FFE AND DFE COEFFICIENTS TO RU.
IN CU
1124
CONVOLVE
SE CIRCUIT
WITH
OLD
COEFFICIENTS
AND LOAD NEWLY
CALCULATED
COEFFICIENTS
INTO RU
XMTR PRECODE
FILTER
RU
TRANSPARENCY VALUES
1126
CU SETS COEFFICIENTS OF PFE 765 AND DFE 820 TO FOR RECEPTION OF UPSTREAM PAYLOAD DATA.
54B
53B

FIG. 45B

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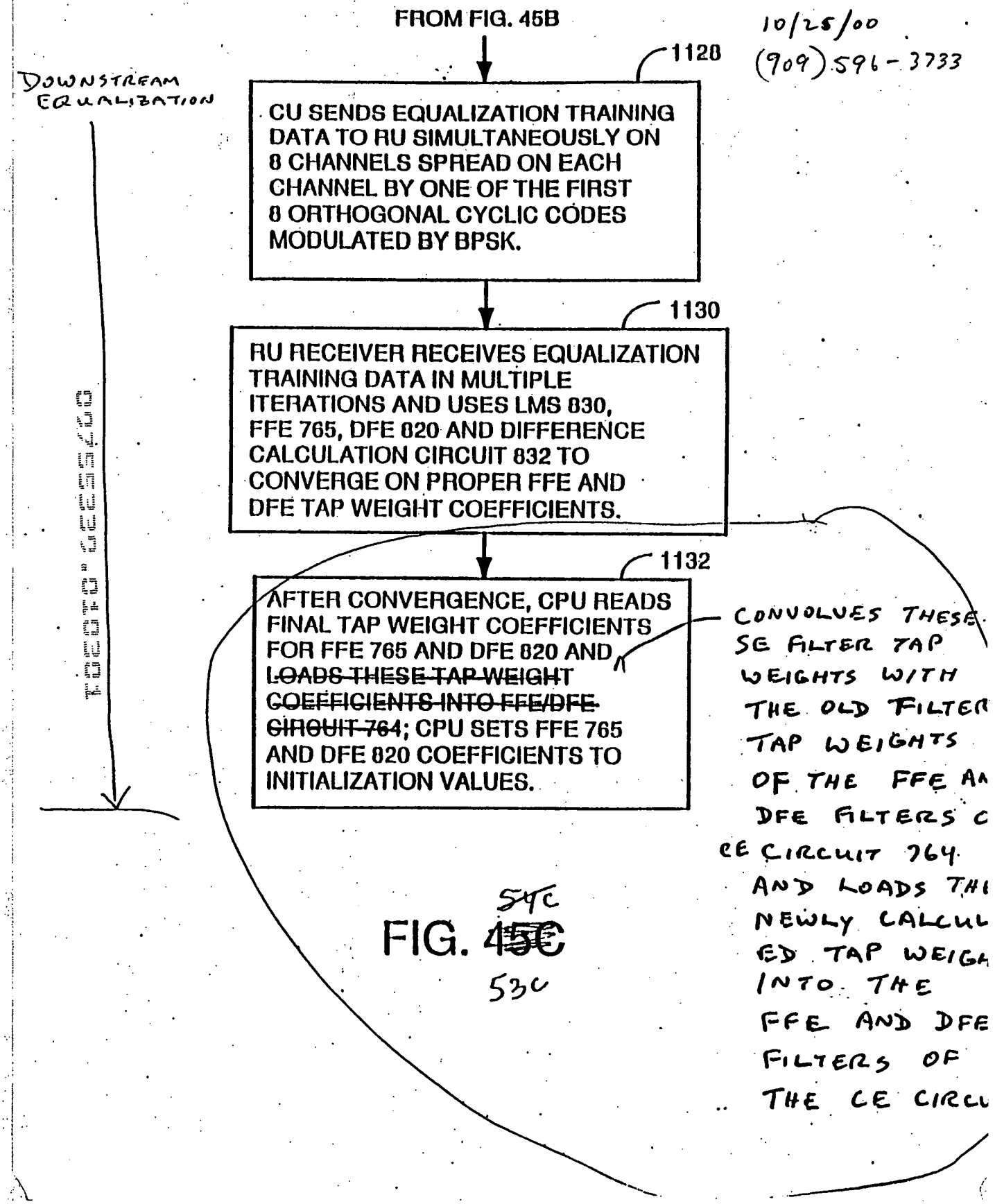
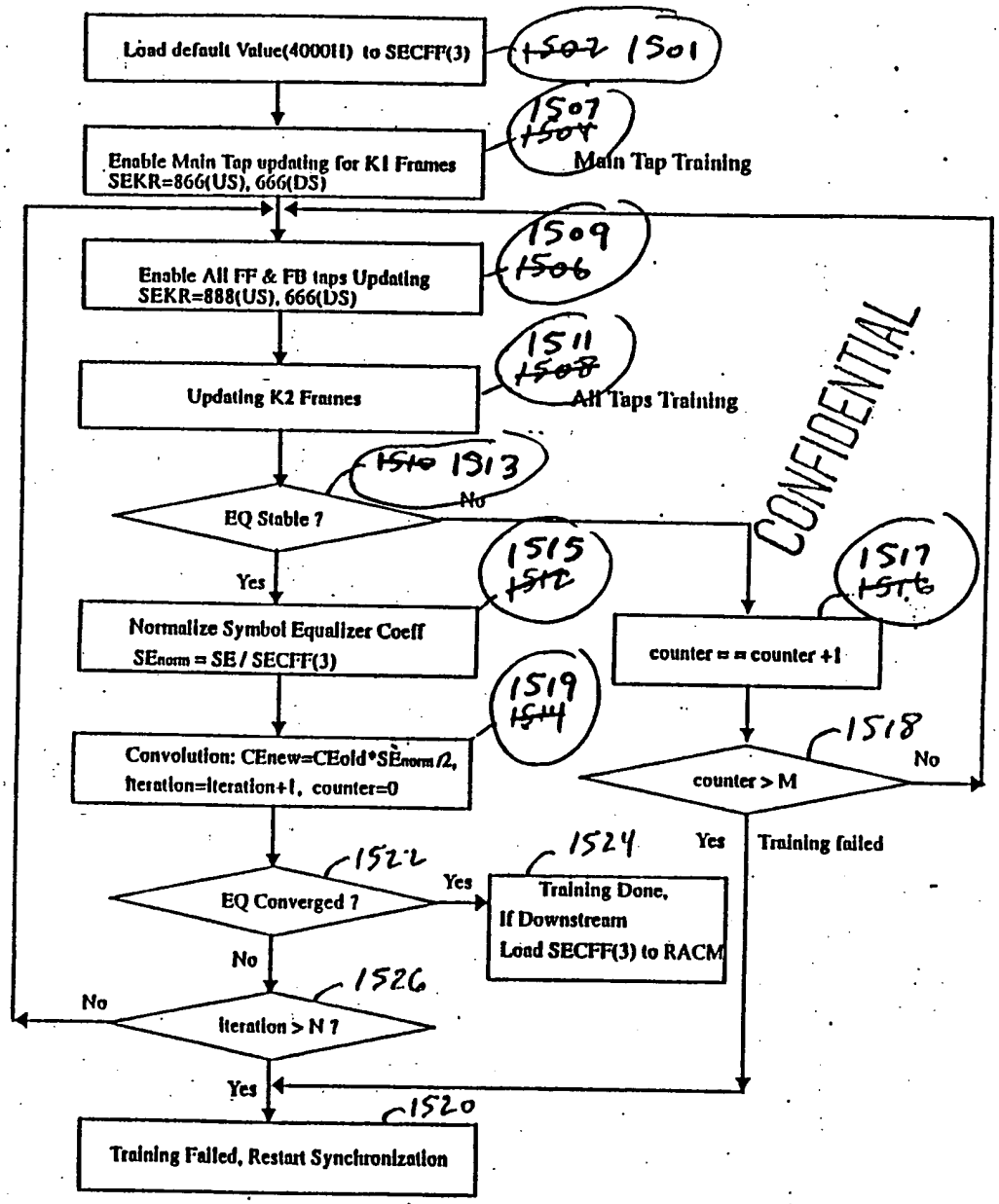


FIG. ~~45C~~ 54C 53C

Initial 2-Step Training Algorithm



2-STEP INITIAL EQUALIZATION TRAINING

FIG. 60